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2017 AUTOMOTIVE EMC GUIDE

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REFERENCE SECTION

INTRODUCTION

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A few years ago, I was on a flight from Boston returning back home to Colorado and found myself sitting next to a farmer from the mid-west. We started chatting about this and that and the conversation eventually turned to farming - a subject in which I was not very well versed.

I commented on the typical round fields prevalent here in the U.S. and how it must be difficult to care for and harvest the crops, as the tractor would have to make continual turns. Actually, he said, "these days our tractors are guided by GPS. All we do is sit in the cab and monitor things." Well, that was eye-opening for me. We talked more about the technology of farming and he briefed me on how satellite imagery and computing tools now help manage fertilization and irrigation. I guess the days of farming past are long gone.

Well, that was "yesterday". Farming today is poised to make a leap to completely autonomous, cloud-based, and computer-controlled tractors and harvesting vehicles. In fact, the technology may be even more advanced than automobiles. CNBC[1] reported that the "Agtech" sector has invested $1.8B in various harvesting and packaging robotics and autonomous vehicle technology during 2016.

Automated tractors (Figure 1) are smaller and lighter than the heavier machinery used today. According to Goldman Sachs, a fleet of smaller automated tractors could lift farmer revenue by more than 10 percent and reduce farm labor costs. Some see these smaller tractors working in groups of five or more in a swarm-like action with dealers renting them out as needed. Farm machinery manufacturer, CNH Industrial (Case IH), has produced quite an interesting video[2] showing a combination of real-life and computer-generated farming concepts that is worth viewing!

Figure 1 - CNH Industrial's concept autonomous tractor can perform a number of agricultural duties, including driving out to a particular field, performing a task, and driving back to the barn. Be sure to watch the video in the References Image, courtesy CNH Industrial.

Mining, as well, has long embraced the concept of autonomous vehicles. OEM Off Highway[3] reports that OEMs such as Caterpillar, Komatsu and Volvo have been developing and testing autonomous vehicle technologies for several years, including both semi- and fully-autonomous machines.

Caterpillar Inc. has fully autonomous mining truck fleets operating at two mines in Western Australia - an iron ore mine operated by BHP Billiton and one by Fortescue Metals Group. Fortescue has 45 Cat 793F CMD trucks running at its mine, which is currently the only fully autonomous commercially available machine Caterpillar currently offers.

Figure 2 - An autonomous haul truck in operation at Rio Tinto's West Angeles mine site in western Australia. Image, courtesy Robe River Iron Associates.

All of the autonomous machines use the Cat MineStar System, Caterpillar's mine operations and mobile equipment management system. Within this system are various features for fleet tracking, proximity detection, remote machine operation, as well as the capabilities for semi- and fully-autonomous operation.

A map of the entire mine and all possible haulage routes is built into the system, and is continuously updated in real time as the trucks complete their loading and dumping cycles. Each autonomous truck is equipped with GNSS hardware and software for accurate guidance along the haul road, loading and dumping areas. All onboard systems communicate with a central control system where operators monitor the fleet and take over control when necessary, such as if a breakdown or blockage of the haul road occurs.

Despite all this technology in current use, the major difference is that these farming and mining machines do not use the public highways, avoiding both the obvious safety and ethical decisions required for on-highway use.

I believe self-driving vehicles will eventually become mainstream, but at a much slower pace than the above examples.

From an EMC point of view, all this new self-driving highway vehicle technology, system infrastructure, and vehicle-to-vehicle control technology will require extensive design, simulation, and testing. New equipment for evaluating radar, Lidar, intra-vehicle, and vehicle-to-vehicle command and control will be required.

We EMC design and test engineers will be required to learn new technologies and test methods for the 70 GHz anti-collision radars, the laser-ranging Lidar, new 5G vehicle-to-vehicle communications, and the myriad of on-board vehicular control and command systems required. All these systems need to "play well" together, or we could potentially see unthinkable carnage on the roadways. As ever, we at Interference Technology will stay at the forefront of this technology and help keep you informed of the latest trends and test requirements.

References:

[1] *CNBC, Future of farming: Driverless tractors, ag robots, 9/2016. http://www.cnbc.com/2016/09/16/future-of-farming-driverless-tractors-ag-robots.html*

[2] *Case IH, The CNH Industrial Autonomous Tractor Concept (Full Version) https://www.youtube.com/watch?v=T7Os5Okf3OQ*

[3] *1 OEM Off Highway, The Growing Potential for Fully Autonomous Mines, http://www.oemoffhighway.com/electronics/smart-systems/automated-systems/article/12243110/autonomous-mining-equipment*

EMC EQUIPMENT MANUFACTURERS CHART

The following chart is a quick reference guide of test equipment and includes everything you'll need from the bare minimum required for key evaluation testing, probing, and troubleshooting, to setting up a full in-house precompliance or full compliance test lab. The list includes amplifiers, antennas, current probes, ESD simulators, LISNs, near field probes, RF signal generators, spectrum analyzers, EMI receivers, and TEM cells. Equipment rental companies are also listed. The products listed can help you evaluate radiated and conducted emissions, radiated and conducted immunity and a host of other immunity tests, such as ESD and EFT.

EMC Equipment Manufacturers		Type of Product/Service												
Manufacturer	Contact Information - URL	Antennas	Amplifiers	Near Field Probes	Current Probes	Spectrum Analyzers/EMI Receivers	ESD Simulators	LISNs	Radiated Immunity	Conducted Immunity	Pre-Compliance Test	TEM Cells	Rental Companies	RF Signal Generators
A.H. Systems	http://www.ahsystems.com	X	X		X						X			
Aaronia AG	http://www.aaronia.com	X	X			X					X			
Advanced Test Equipment Rentals	https://www.atecorp.com	X	X			X	X	X	X	X	X		X	X
Amplifier Research (AR)	https://www.arworld.us/	X	X			X		X	X	X	X			X
Anritsu	http://www.anritsu.com					X					X			X
Beehive Electronics	http://www.beehive-electronics.com			X							X			
Electro Rent	http://www.electrorent.com		X			X	X	X	X	X	X		X	X
EM Test	http://www.emtest.com									X	X	X		
EMC Partner	https://www.emc-partner.com						X			X				
Empower RF Systems	http://www.empowerrf.com		X						X					
Emscan	http://www.emscan.com										X			
ETS-Lindgren	http://www.ets-lindgren.com	X	X	X	X			X	X	X	X	X		X
Fischer Custom Communications	http://www.fischercc.com			X	X			X			X			
Gauss Instruments	https://www.gauss-instruments.com					X								
Haefley-Hippotronics	http://www.haefely-hipotronics.com						X			X				
Instrument Rental Labs	http://www.testequip.com		X			X	X	X	X	X	X		X	X
Instruments For Industry (IFI)	http://www.ifi.com		X						X	X				
Keysight Technologies	http://www.keysight.com			X		X		X			X			X
Microlease	https://www.microlease.com		X			X	X	X	X	X	X		X	X
Milmega	http://www.milmega.co.uk		X						X	X				
MVG	http://www.mvg-world.com	X												
Narda/PMM	http://www.narda-sts.it	X	X			X		X	X	X	X			
Noiseken	http://www.noiseken.com						X			X	X			
Ophir RF	http://ophirrf.com		X							X				
Pearson Electronics	http://www.pearsonelectronics.com				X									
Rigol Technologies	https://www.rigolna.com			X	X	X					X			X
Rohde & Schwarz	https://www.rohde-schwarz.com	X	X	X	X	X		X	X	X	X			X
Siglent Technologies	http://siglent.com/			X		X					X			X
Signal Hound	https://signalhound.com			X		X					X			X
TekBox Technologies	https://www.tekbox.net		X	X				X			X	X		
Tektronix	http://www.tek.com			X		X					X			
Teledyne LeCroy	http://teledynelecroy.com				X				X	X	X			
Teseq	http://www.teseq.com		X		X		X		X	X	X	X		
Test Equity	https://www.testequity.com/leasing/		X			X	X	X	X	X	X		X	X
Thermo Keytek	https://www.thermofisher.com						X			X				
Thurlby Thandar (AIM-TTi)	https://www.aimtti.com					X					X			X
Toyotech (Toyo)	https://toyotechus.com/emc-electromagnetic-compatibility/	X	X			X		X	X		X			
TPI	http://www.rf-consultant.com													X
Transient Specialists	http://www.transientspecialists.com								X	X		X		
TRSRenTelCo	https://www.trsrentelco.com	X	X			X		X	X	X	X		X	X
Vectawave Technology	http://vectawave.com		X											
Windfreak Technologies	https://windfreaktech.com													X

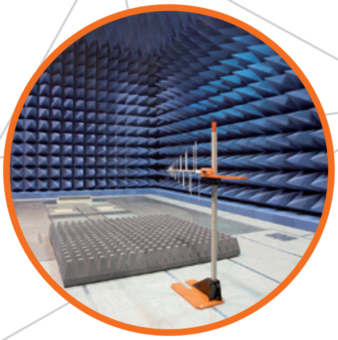
FLEXIBLE EMC TEST AND MEASUREMENT SOLUTIONS

Can I Perform **EMC and Antenna Measurement** Testing in the Same Chamber?

YES you can. In general, EMC testing covers lower frequencies requiring specialized hybrid solutions, while antenna measurement testing covers higher frequencies, higher accuracies, tighter positioner tolerances, and better overall absorber isotropy and performance.

Here are some factors to take into account when considering one chamber for combined testing vs two separate chambers:

- **Frequency range of each type of testing**
- **EUT and AUT sizes**
- **Required far-field distances of antenna measurement testing**
- **Relative QZ performance requirements**
- **Mechanical tolerances of the positioners**
- **Types and performance of absorber required**



The choice of a combined chamber or separate chambers depends on the specifications and on expectations that need to be weighed.

Our team at MVG can help you in making the right decision. We design, manufacture, and install shielded enclosures, anechoic chambers, shielded doors, absorbers and more.

Whether it be EMC testing, antenna measurement testing, or both, MVG ***can help you evaluate and choose the best solution for your needs.***

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USING AN OSCILLOSCOPE TO VERIFY EMC TESTS FOR AUTOMOTIVE ELECTRONICS

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Consumer demand for more entertainment, safety, and communication options within automobiles has significantly increased both the density of electronic components and the number of on-board wired and wireless signals. The result: an ever-expanding range of signals contained within the same car-sized fixed space.

USING AN OSCILLOSCOPE TO VERIFY EMC TESTS FOR AUTOMOTIVE ELECTRONICS

It's important for electronic components used within automobiles to be robust and to function correctly in a real-world environment increasingly filled with electromagnetic (EM) waves originating from cell phones, Bluetooth headsets, satellite radio, AM/FM radio, wireless internet, RADAR, and countless other potential sources of electromagnetic interference (EMI). Ensuring robustness means meeting rigorous EMI immunity standards within a controlled environment. Electronic Control Units (ECUs) under test typically must comply with strict ISO (International Organization for Standardization) guidelines and with requirements negotiated between the automobile manufacturer and the ECU component supplier.

As an example of typical frequencies and field strengths seen during testing, consider the radiated RF immunity test described in ISO/IEC 61000-4-21. The test utilizes a reverberant chamber containing a mechanical-mode tuner. When a sufficient number of tuner positions have been obtained at a given test frequency, the tuner produces a statistically uniform field within the useable volume of the chamber with test frequencies ranging from 0.4 to 3 GHz and field strengths as high as 200 V/m (CW and AM) and 600 V/m (radar pulses). Field strengths in such test environments are too high, both for electronic test equipment to monitor the signals, and for test personnel to be safely within the reverberent chamber. Thus, measurement instruments and test personnel remain outside of the sealed chamber. Fiber-optic transmitter and receiver units and fiber optic cables transport the signal from the ECU inside of the chamber to the test equipment outside of the chamber.

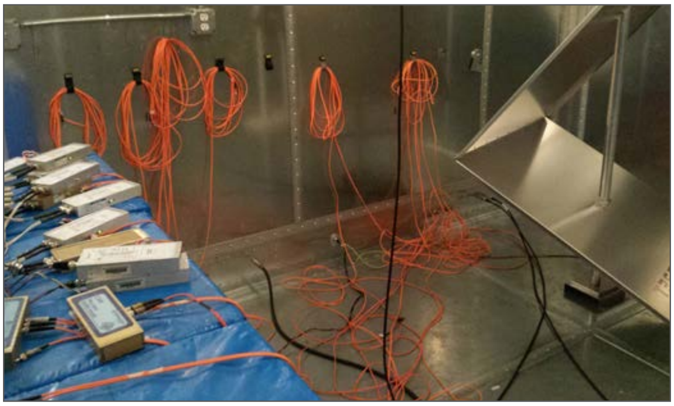


Figure 1: Reverberant chamber equipped with a mode tuner (right) and fiber optic transmitters (left). Note that the ECU and antennas were present also, but are not shown in this photo.

Figure 1 shows a real-world test configuration for deviation detection in immunity testing, photographed from inside the sealed chamber (while the transmitting antenna was powered off). Note that the mode tuner is shown to the right of the chamber. The left side of the chamber has CAN bus fiber-optic transmitters placed on a foam bench having a relative permittivity of < 1.4 and located within the usable volume of the reverberant chamber. The fiber-optic transmitters optically convert the output signals from the ECU under test. The signals are transported through the chamber by means of RF-hardened fiber-optic cables that exit the chamber near the floorboard via waveguides.

In addition to immunity to EMI, automotive electronic components are designed to have a certain level of immunity to ESD. Test levels for ESD immunity range from 2 kV to 25 kV. Voltage is typically applied in steps until it reaches an established limit. Before an ESD simulator is applied to the ECU under test, it must first be calibrated using an oscilloscope. *Figure 2* shows an ESD simulator gun applying a contact discharge into a current shunt target that is connected to the oscilloscope's 50Ω DC-coupled input via a double-shielded cable and inline attenuators.

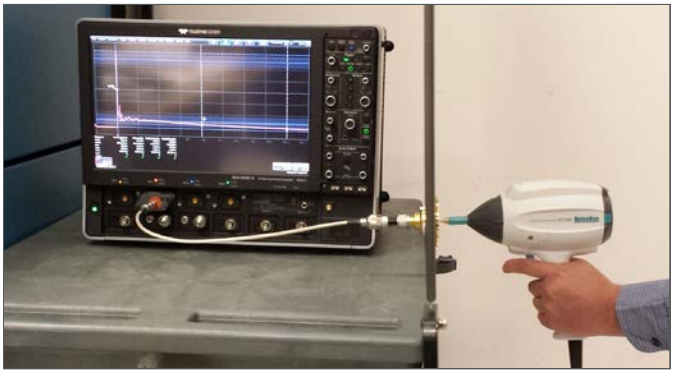
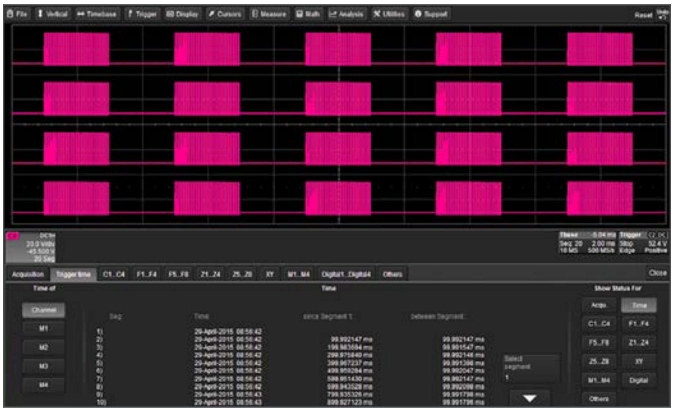


Figure 2: An ESD gun discharges into a current shunt target. The resulting pulse waveform is captured and measured with an oscilloscope.

Verifying the ESD simulator includes characterizing the discharge pulse waveform. The second edition of ISO 10605 identifies rise time, first peak current, current at t1, and current at t2 as the parameters of interest. The values of t1 and t2 vary with the value of R and C in a given RC network for the purpose of verifying its time constant. An oscilloscope rapidly and automatically characterizes each of these measurement parameters.

Another important measurement requirement for automotive electronics is the Electrical Fast Transient (EFT), a phenomenon in which current flow is instantaneously interrupted, resulting in arcing between contacts. Common causes for EFT can include relay-contact bounce, opening and closing of circuit breakers, switching of inductive loads, and powering down equipment. Breakdown of the air gap between electrical contacts often triggers a rapid burst of EFT pulses. The sudden sequence of energy bursts from EFT pulses can couple into nearby electrical paths, risking digital signal corruption of automotive electronic systems and ensuing potential malfunctions. Therefore, electronic products must be tested to ensure safe operation in the presence of EFT events.

Figure 3 depicts a series of EFT bursts acquired as segments using an oscilloscope's sequential capture mode. Note that the long gap time between bursts has been removed by the process of sequential capture, leaving only the desired burst waveform within the acquisition.



Seg	Time	since Segment 1	between Segment
1)	29-April-2015 08:56:42		
2)	29-April-2015 08:56:42	99.992147 ms	99.992147 ms
3)	29-April-2015 08:56:42	199.983694 ms	99.991547 ms
4)	29-April-2015 08:56:42	299.975840 ms	99.992146 ms
5)	29-April-2015 08:56:42	399.967237 ms	99.991398 ms
6)	29-April-2015 08:56:42	499.959284 ms	99.992047 ms
7)	29-April-2015 08:56:42	599.951430 ms	99.992147 ms
8)	29-April-2015 08:56:42	699.943528 ms	99.992098 ms
9)	29-April-2015 08:56:43	799.935326 ms	99.991798 ms
10)	29-April-2015 08:56:43	899.927123 ms	99.991796 ms

Figure 3: EFT bursts acquired as segments and time stamped

In contrast, *Figure 4* shows EFT pulses, rather than bursts, acquired as segments.

Potentially tens of thousands of individual pulses could be acquired. Note that the time scaling for sequential burst capture here is 2 ms per division (corresponding to a 20-ms time capture window), while the time scaling for sequential pulse capture is 100 ns per division (corresponding to a 1-ms time capture window).

Seg	Time	since Segment 1	between Segment
1)	29-April-2015 09:01:44		
2)	29-April-2015 09:01:44	100.002 µs	100.002 µs
3)	29-April-2015 09:01:44	200.002 µs	100.000 µs
4)	29-April-2015 09:01:44	300.001 µs	100.000 µs
5)	29-April-2015 09:01:44	400.002 µs	100.000 µs
6)	29-April-2015 09:01:44	500.051 µs	100.049 µs
7)	29-April-2015 09:01:44	600.051 µs	100.000 µs
8)	29-April-2015 09:01:44	700.051 µs	100.000 µs
9)	29-April-2015 09:01:44	800.050 µs	99.999 µs
10)	29-April-2015 09:01:44	900.050 µs	100.000 µs

Figure 4: EFT pulses acquired and time stamped as segments

The intersegment time stamps in EFT burst capture mode shows an inter-burst timing of approximately 100 ms between bursts, while the intersegment time stamps in EFT pulse capture mode shows an inter-pulse timing of approximately 100 ms between pulses. The time scaling between the two captures differs by a factor of 1000x, highlighting the contrast between the characterizations of either individual EFT pulses or EFT bursts.

A final consideration is voltage drop and interruption testing. To verify that devices will operate properly in the presence of a voltage supply interruption, electronics must be tested for voltage dips (defined as a sudden reduction in voltage followed by recovery to the original voltage), short interruptions (defined as a complete absence of supply voltage for a short period of time followed by a recovery to the original voltage), and voltage variations (defined as gradual changes of the supply voltage to a higher or lower voltage value than the rated voltage).

To ensure that the signal generator outputs the intended conditions to simulate these effects, the signal generator waveform characteristics must be validated with an oscilloscope before connecting the generator to the electronic units under test.

Figure 5 shows an example (abbreviated) waveform from the standard ISO 16750-2. This waveform shape is used to verify the reset behavior of devices with reset functionality (such as microcontrollers) at different voltage drops. Note that the waveform begins at 13.55 V. In the first dip, the voltage level drops approximately 10.6% to 12.12 V where it dwells for 105 ms, then the level returns to its original 13.55-V battery level. One half second later, the second dip lowers the voltage level 21.2% to 10.68 V, where it dwells for 105 ms before returning to the original 13.55 V. This process of decrementing the voltage-dip level and returning to source voltage continues at fixed intervals until the level reaches zero volts.

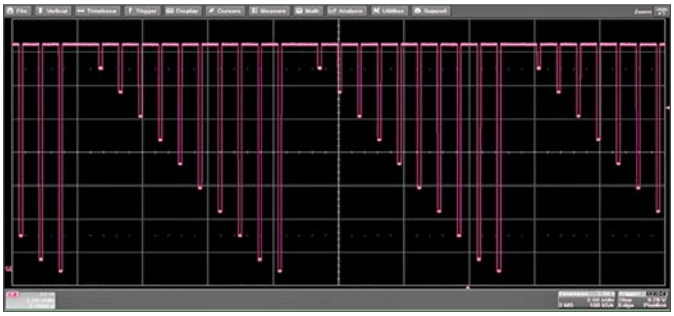


Figure 5: Signal used for testing below-battery voltage levels.

Testing the time duration and voltage level reduction of each dip is a time-consuming and error-prone task when relying on a live operator to measure using cursors from a single waveform capture. Not only do cursors rely on the operator's hand-eye coordination, but they are also specified to yield a 2% measurement inaccuracy. In addition, significant time is lost as an operator manually places each cursor at the correct time and voltage level. Lastly, the results will cover only a single acquisition, which by definition does not provide statistical significance.

Figure 6 shows a measurement method that resolves each of the problems listed above. With this method, we use a negative going runt trigger to isolate a specific dip level. A runt trigger is a hardware trigger selection in which the waveform must first pass through one threshold, but not cross through a second threshold, to meet the trigger criteria. By selecting the runt polarity to be negative going, the trigger circuit isolates a voltage dip, which meets the criteria. Because the trigger circuit can lock onto this specific dip level each time it occurs, the oscilloscope rapidly accumulates measurement statistics. In *Figure 6*, the trigger circuit has locked onto the first dip. With display persistence turned on, one can see that the first dip is the only dip acquired by the oscilloscope (*Figure 6*, right, pink). A histogram further displays quantified results with statistical significance. In this case, the histogram plots the distribution of pulse width along the X-axis, with the number of occurrences of each width displayed on the Y-axis (*Figure 2*, right, blue). Statistics showing measurement results are tallied in the measurement parameter table (*Figure 6*, right, bottom).

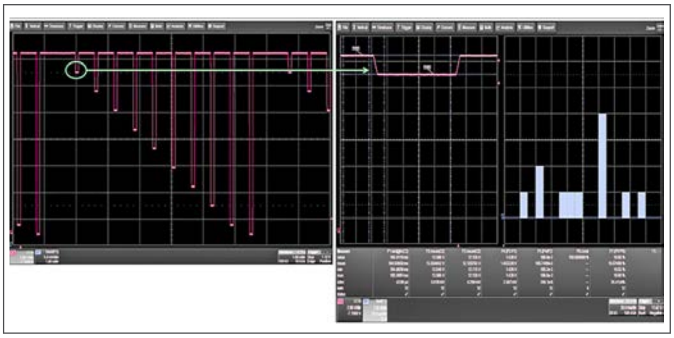


Figure 6: Runt trigger, measurement parameters and histogram quantify the first dip both in terms of voltage and percent

Automotive EMI and ESD testing involves many forms of testing. Oscilloscopes are well equipped to perform the rapid parametric measurements required for EMC immunity testing as well as calibration of an ESD simulation simulator. Using a fast-segmented acquisition mode, both electrical fast transient pulses and bursts can be captured and characterized. New techniques have been developed for validating the setup for voltage drop tests, providing rapid and accurate characterization.

Note: Photographs and images used in this article appear courtesy of Hitachi Automotive Systems, Farmington Hills, MI (an ISO-accredited lab).

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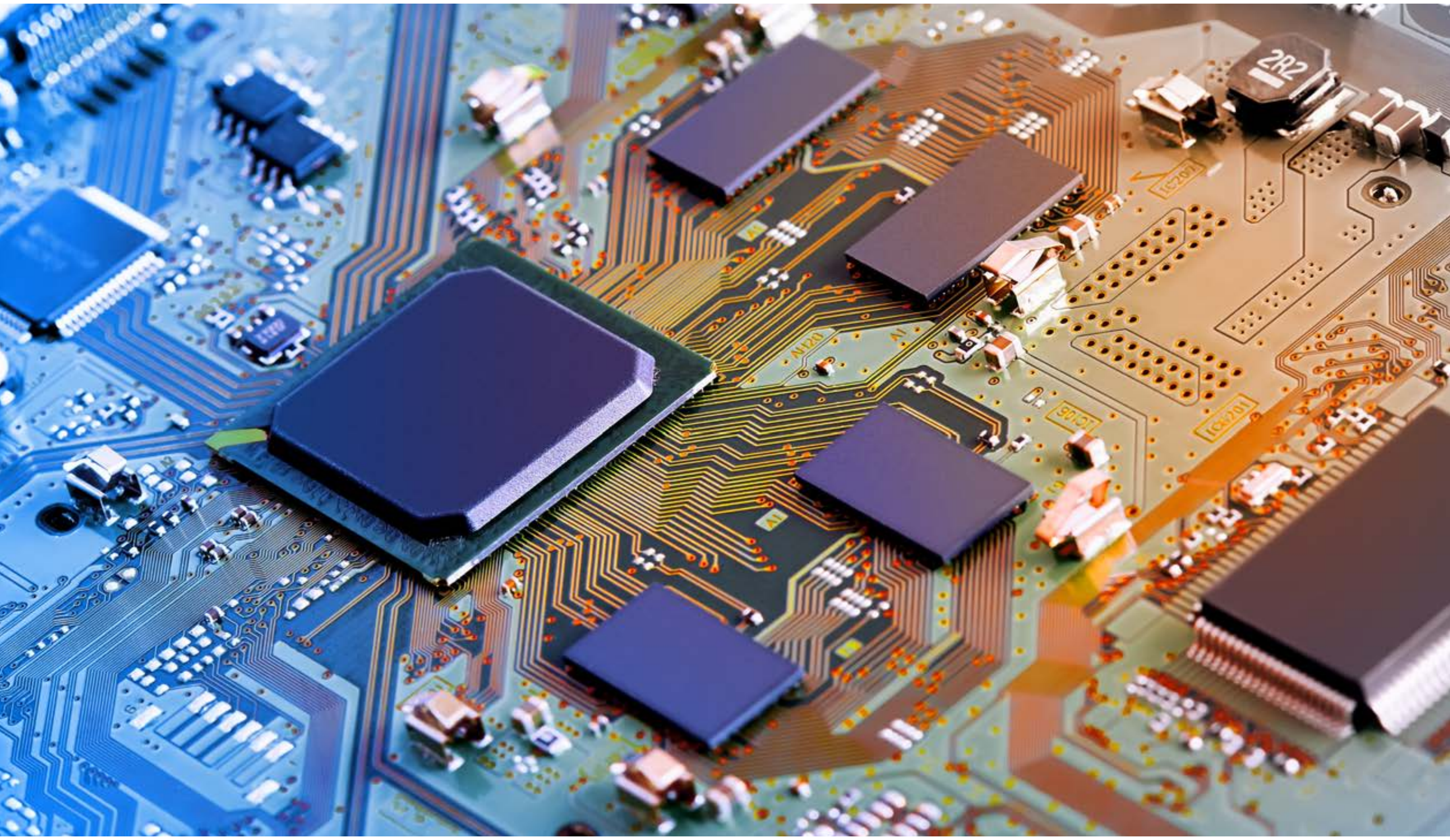
CHOOSING AND USING SILICON PROTECTION DEVICES

Dave Rose

Correctly choosing an external (off chip) Transient Voltage Suppressor (TVS) is not as simple as it once was. Integrated Circuit (IC) feature size is shrinking (Figure 1) and more and more inputs are being exposed to the outside world. Portable consumer devices are everywhere and have more functions in smaller and smaller sizes, necessitating smaller and smaller TVS packaging. At the same time, the demand for bandwidth is sky-rocketing, as witnessed by three popular technologies: Ethernet, HDMI and USB (Figure 2).



CHOOSING AND USING SILICON PROTECTION DEVICES

System Level Considerations

Failure Levels of Unprotected Inputs

The first constraint to be considered is the failure level of the input to be protected. Hopefully, this will be known based on Transmission Line Pulse (TLP) or Human Body Model (HBM) testing, but this is often not the case. If it is not known, and cannot be measured, a reasonable estimate must be made.

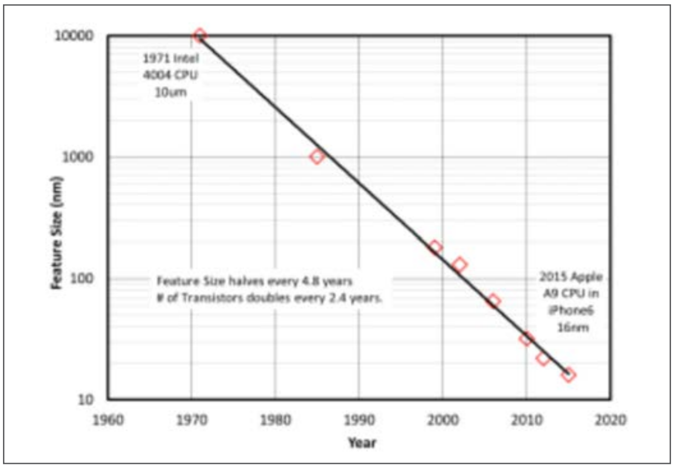


Figure 1: Process Node Trends

Symbol Rate

The symbol rate of the application must be known. This is not always the same as the bit rate. For complex modulation schemes, the number of bits per symbol can be much larger than one. In some simple modulation schemes the number of bits per symbol can be less than one. Typically, the analog bandwidth required for a digital signal is between half the symbol rate and the symbol rate. For example, if a digital protocol requires a symbol rate of 5Gsymbols/s, then the analog bandwidth required is between 2.5GHz and 5GHz depending on channel noise and other factors.

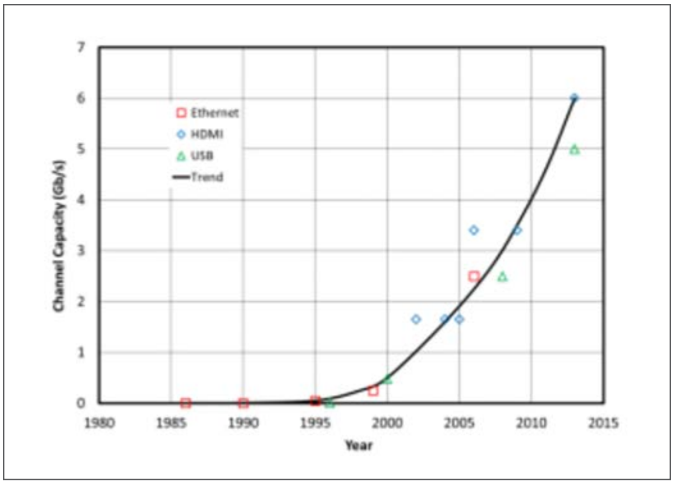


Figure 2: Channel Capacity Trends

System Protection Level Requirements

The requirements for system level protection must be known and understood. There is a huge difference between a person shuffling across a carpet with a smart phone and a 10G Ethernet Inter-Building Cable subjected to a near lightning strike. There are standards available for all likely Electrostatic Discharge (ESD) and surge threats; these should be used along with applicable protection device datasheets to determine a good protection scheme.

Protection Device Considerations

Insertion Loss

Any device added to a communication channel will introduce extra signal losses in that channel. These losses are caused by the parasitics of the added device. Often, only the capacitance is considered, but especially for low capacitance devices, the stray inductance has a very large effect. *Figure 3* shows a comparison between a measured part, a full model simula tion for the part, and a simulation using only the part's junction capacitance. It is quite apparent that there is a large difference even well below the -1dB point.

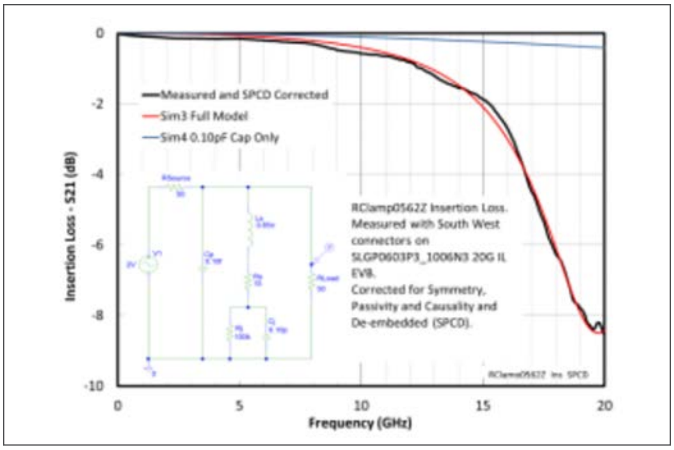


Figure 3: Insertion Loss Comparison

Using Silicon TVS Diodes

Silicon TVS diodes have been used for many years as protection devices. They consist of one or more TVS diodes and possibly one or more steering diodes. Capacitance can cover two orders of magnitude or more; there really is no typical, nor a typical reduction magnitude. The steering diodes are used to reduce capacitance and, in a bridge configuration, allow a uni-directional TVS to symmetrically clamp in a bi-directional fashion.

The TLP characteristic of the TVS protection device must include very low leakage at the maximum port voltage (VRWM) and the clamping voltage at the Required Human Metal Model (HMM) protection level must be lower than the Human Body Model (HBM) on-chip protection Failure Voltage, as shown in *Figure 4*. With increasing frequencies and decreasing on-chip protection levels, it has become more difficult to satisfy both of these criteria while still meeting insertion loss, size and cost requirements.

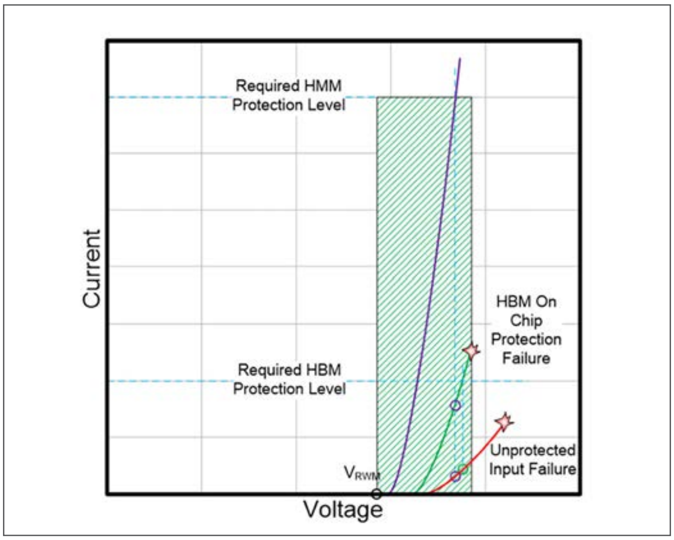


Figure 4: Zener Type Protection

Using Snap-Back Devices

Snap-back devices can either be of the shallow snap-back or deep snap-back types. An example of a Shallow Snap-Back device would be a Bipolar Transistor (BJT) especially designed for enhanced collector-emitter punch-through breakdown. These devices exhibit low capacitance for their protection levels and are very good for protection in the 1.5V to 4V working range. Deep snap-back devices are typically a 4-layer PNPN SCR type structure. A much larger "window" is available for the external protection device *Figure 5*.

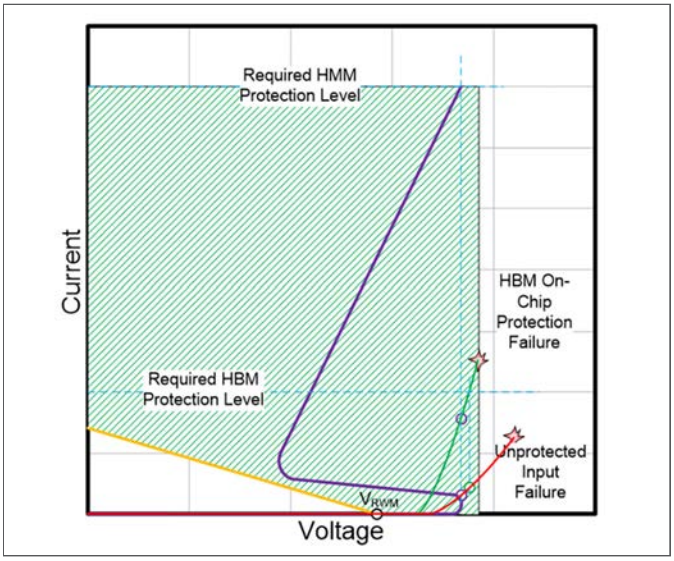


Figure 5: Snap-Back Protection

Avoiding Latch-Up

The major concern for snap-back protection is the avoidance of latch-up. Latch-up can occur if the protection device enters its snap-back region and sufficient DC current is sourced into the protected line to hold it there. Most typically, this occurs due to pull up resistors on the signal line.

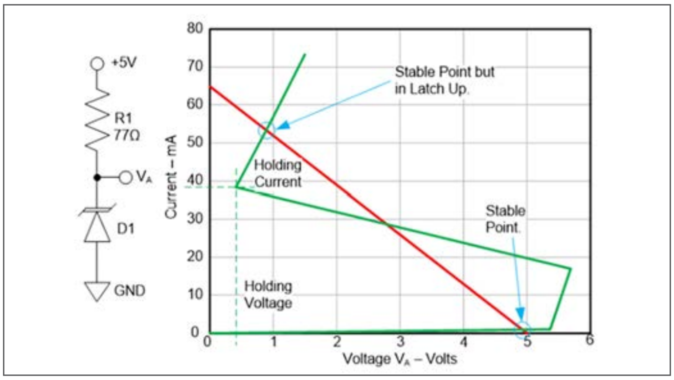


Figure 6: Snap-Back and Load Line

Figure 6 shows an illustration of the problem. The red line is the locus of the operating points of the resistor R1, note that the X-axis is VA – the voltage at the node where the resistor and protection device connect. The green line is the locus of the operating points of the protection device. There are three points where the loci coincide: The first is just below 5V before the protection device turns on and is the normal maximum operating point; the second is at about 2.8V, but is unstable since the total resistance is negative; and the final point is at slightly less than 1V and is the latch-up point.

When a transient event occurs, a high current pulse will flow through the protection device, as the transient fades, the current in the protection device will fall until it reaches the latch up point and will not be able to fall any further. The input will be latched up and will be unresponsive to normal signals. The only way to get out of latch-up is to momentarily pull the VA node low or to cycle system power.

Latch-up can be avoided with proper design. All that needs to be done is to ensure the second and third crossing points do not exist by careful selection of either pull-up resistor or the protection devices holding current and voltage.

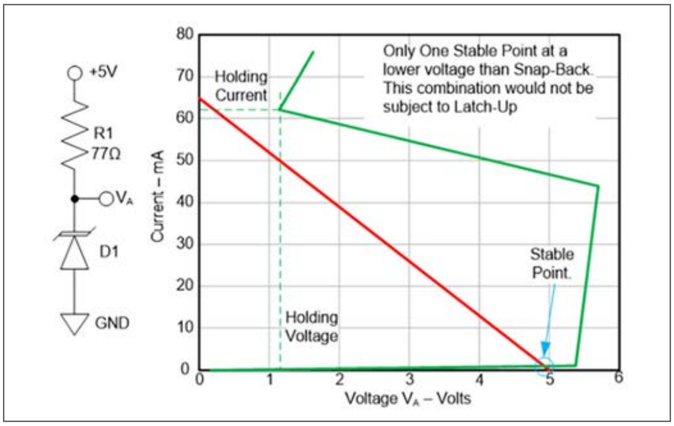


Figure 7: Avoiding Latch-Up

Other Considerations

Board Layout

The best protection device in the world will not be able to do its job properly if the board layout is not optimum.

Guidelines for proper board layout include:

1. Protect at the system input, i.e. generally, the protection device should be as close as possible to the connector where any transient event might be injected.

2. Use Kelvin like connections to avoid adding spikes due to parasitic inductance (*Figure 8*).

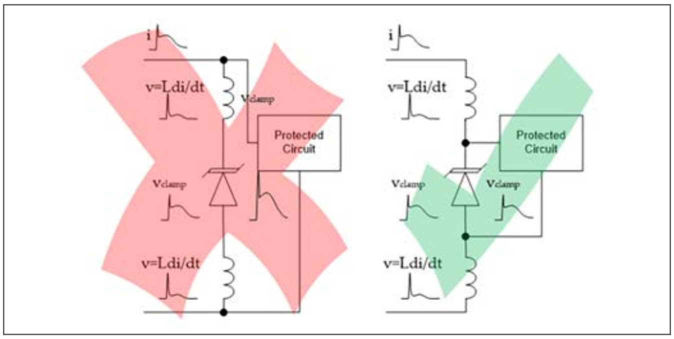


Figure 8: Minimizing parasitic inductance effects

3. Minimize any opportunities for coupling. Avoid routing the protected circuitry close to the protection circuitry. Take care with ground planes to ensure return currents are properly controlled. Minimize loop areas to minimize radiation, pickup and inductance, a good practice in any case.

Multi-Line Protection

Multi-line protection packages are becoming more popular and are generally tailored for a particular application. Of course, the packages are larger and generally have slightly higher inductance than an equivalent single line package. Make sure that this extra inductance will not be detrimental in the intended application. The insertion loss curves in the part datasheet will be helpful here. If possible, the signal lines should be made to "flow through" without major directional changes to help maintain proper signal integrity.

Summary

By using a systematic approach, it is relatively straightforward to choose an optimum protection device for a given application by using knowledge of the system and the detailed protection requirements. In most cases, the application is well known and the protection device manufacturer will have a sub-set of their devices already chosen for the application. This will be a good starting point for protection device selection.

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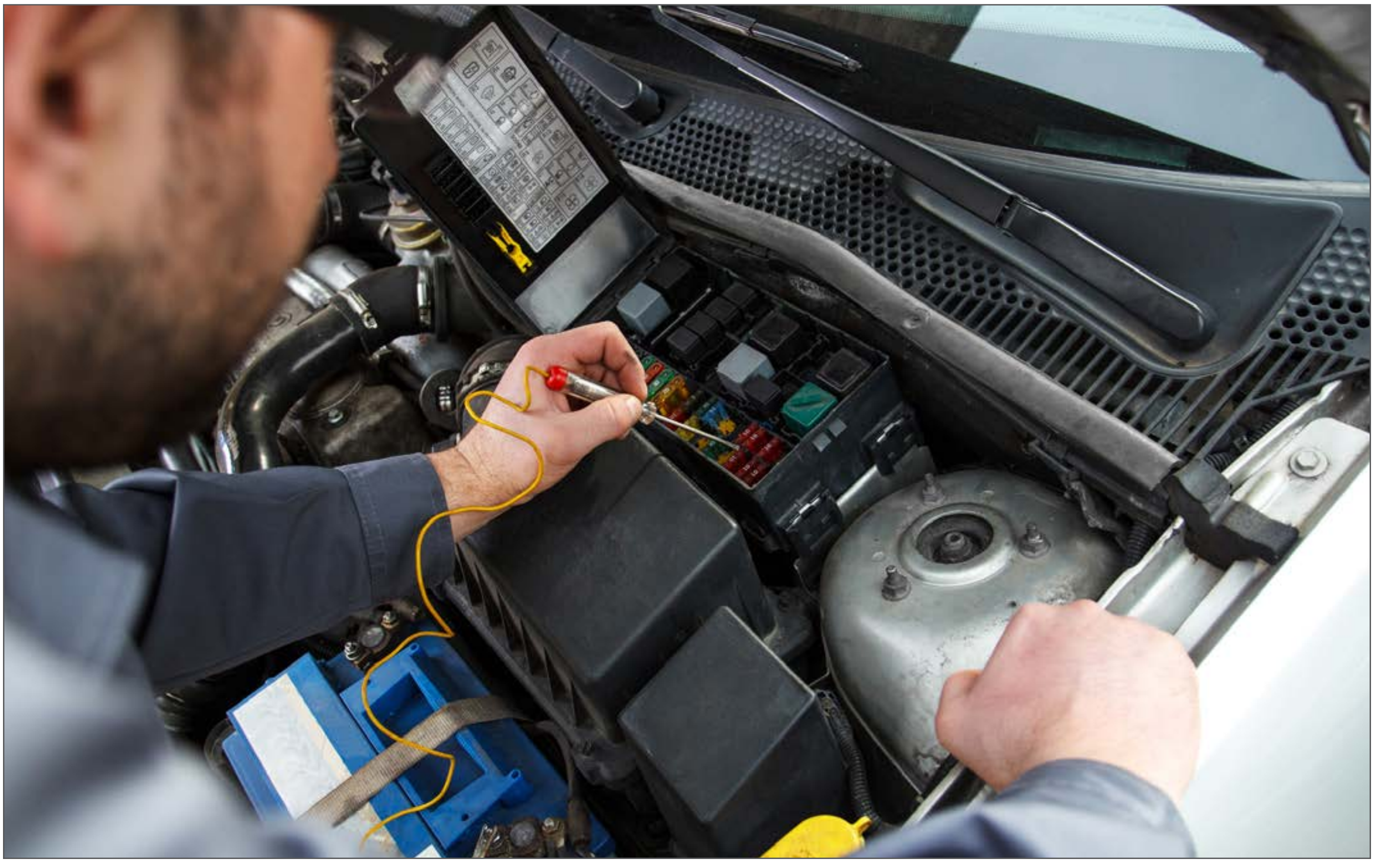

TOP THREE EMI AND POWER INTEGRITY PROBLEMS WITH ON-BOARD DC-DC CONVERTERS AND LDO REGULATORS

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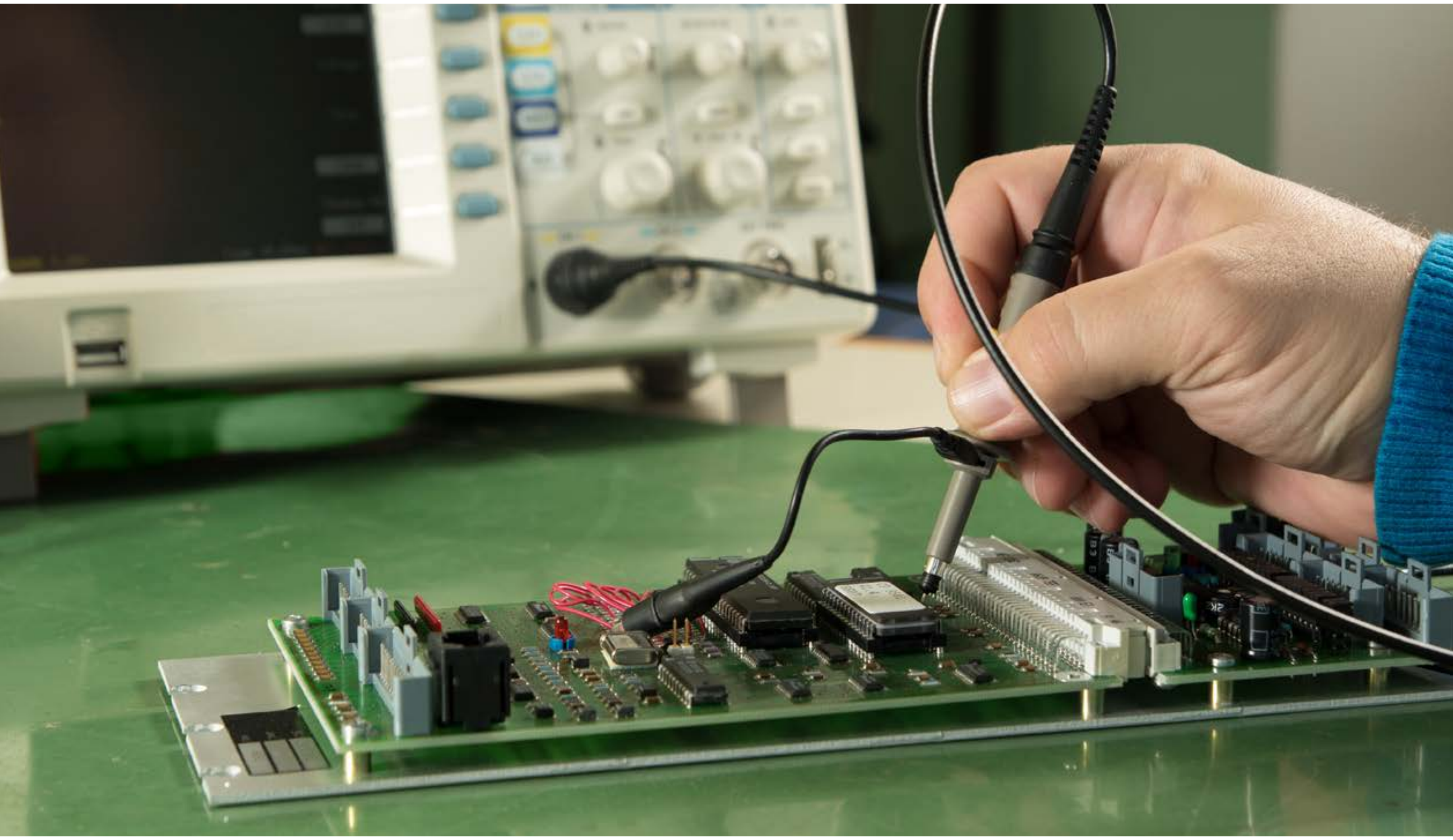
Modern devices are continuing a long-term trend of squeezing more electronics into smaller packages, while also increasing system performance, data rates and operating efficiency. Higher efficiencies are often achieved by implementing faster silicon MOSFETs or even faster eGaN FETs while size is reduced by increasing switching frequencies and replacing aluminum and tantalum capacitors with smaller ceramic devices. One result of this trend is that there is greater interaction between the disciplines of EMI, signal integrity (SI) and power integrity (PI).



TOP THREE EMI AND POWER INTEGRITY PROBLEMS WITH ON-BOARD DC-DC CONVERTERS AND LDO REGULATORS

Introduction

EMI is a measure of the electromagnetic emissions produced by the high-speed current and voltage signals the system creates. Power integrity is a measure of the power quality at the device that being powered. This means that the power supply voltages must be maintained within the allowable operating voltage range of high-speed devices.

Devices, such as modems, reference clocks and low noise amplifiers (LNAs) are all sensitive to noise on the power rails, which results in timing jitter, spurious responses reduced data channel eye openings, and degraded signal-to-noise ratio (SNR). This too, is a measure of power integrity.

The power supply itself is a noise source and the noise sources generated by the power supply must be kept from propagating through the system.

This article discusses the three most common causes of EMI and power integrity issues while providing tips for how to avoid or minimizes them in your design,

1. **Ringing** on switched waveforms causes broad resonant peaks in the emission spectrum.
2. **DC-DC converters generate noise** at the switching frequency, and because of high speed switching devices, can generate broadband switching harmonics well into the GHz.
3. **Power plane resonance** in DC-DC converter or LDO regulators due to high-Q capacitors resonating with power planes.

Ringing and Radiated Emissions

Any ringing on the switched waveform (fairly common) can lead to broadband resonances in the resulting RF spectrum. Resonant frequencies resulting from DC-DC converters or low dropout (LDO) linear regulators can be as low as a few kHz while resonance due to the PDN with switching devices, such as MOSFET's can be in hundreds of MHz or higher.

The harmonic energy resulting from this switching is "captured" by the PDN and device resonances, evident as ringing in the time domain. The current and voltage of this ringing produces EMI. The magnitudes of the ringing and EMI are related to the quality factor (Q) and characteristic impedance of the resonance and the harmonic energy produced by the switching.

As an example, the switching waveform on a DC-DC buck converter demo board was measured with a Rohde & Schwarz RTE 1104 oscilloscope and Rohde & Schwarz RT-ZS20 1.5 GHz active probe (*Figure 1*).

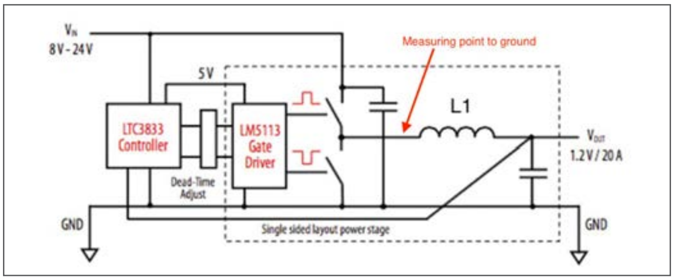


Figure 1. Diagram showing the measuring point at the switch device junction (on the left side of L1) to ground return.

There was a very large ringing superimposed on the switched waveform of 216 MHz. This can be seen clearly in *Figure 2*.

A Fischer Custom Communications F-33-1 current probe was used to measure both the input power cable common mode current (violet trace) and output load differential mode current (aqua trace). See *Figure 3*. Note the broad resonant peaks at 216 MHz (*marker 1*) and the second harmonic at 438 MHz (*marker 2*).

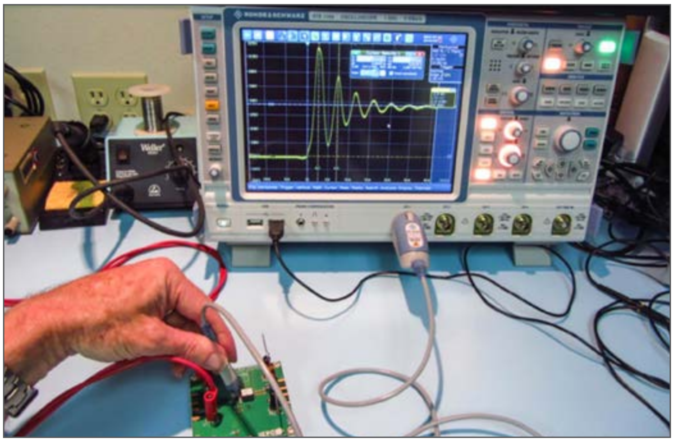
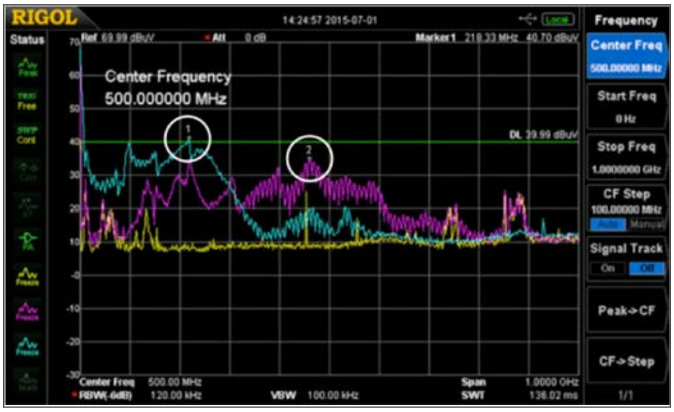


Figure 2. Measuring the rise time and ringing on a DC-DC converter. Notice to strong ringing at 216 MHz.



14:24:57 2015-07-01

Ref 69.99 dBuV Att 0 dB Marker1 218.33 MHz 40.70 dBuV

Center Frequency 500.000000 MHz

DL 39.99 dBuV

Center Freq 500.00 MHz RBW(-6dB) 120.00 kHz VBW 100.00 kHz Span 1.0000 GHz SWT 136.02 ms

Center Freq 500.00000 MHz

Start Freq 0 Hz

Stop Freq 1.0000000 GHz

CF Step 100.00000 MHz Auto Manual

Signal Track On Off

Figure 3. Resulting resonances from the 216 MHz ring frequency (marker 1) and second harmonic at 438 MHz (marker 2).

Remediation Tips - There are several ways to improve the design to minimize the resonances, ringing and therefore EMI. Since the energy is related to the switching frequency, rise time of the switching, characteristic impedance, and Q of the resonances, these factors are also the paths to mitigation.

- Slower edges will degrade operating efficiency but reduce high frequency energy
- Careful PCB design and capacitor selection will minimize the characteristic impedance and Q
- Keep traces short and wide and dielectrics thin.
- Keep all the switching circuitry on one side of the board, preferably with a thin dielectric to the respective ground return plane.
- Use of a snubber circuit, damping of resonances using controlled ESR capacitors, or redesign of the inductor for lower leakage inductance.

For additional detail on measuring ringing refer to *Reference 1*.

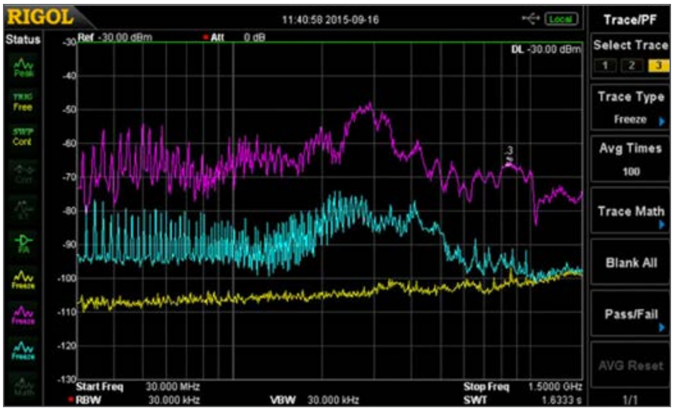
Fast edges create broadband noise at GHz frequencies
Today's on-board DC-DC converters use switching frequencies as high as 3 MHz. This is an advantage because it allows for physically smaller inductor and filter components, as well as increased efficiency. However, the fast edge speeds create broadband harmonic energy. The bandwidth of this harmonic energy is related to the voltage and current rise time. A 1ns edge speed can produce harmonic energy up to 3 GHz, or more.

These broadband harmonics are the cause of radiated emissions failures and also can affect the receiver sensitivity of any on-board telephone modems or other wireless systems, such as GPS. *Figure 4* shows how a typical DC-DC converter circuit can be characterized using an H-field probe connected to a spectrum analyzer.

It's also possible to connect the probe to an oscilloscope and hold it near each DC-DC converter to get some idea of the ringing, if any, without disturbing the circuit.

Figure 4. Probing DC-DC converter noise sources on a typical wireless device.

Figure 5 shows the resulting measurement of a couple DC-DC converters. The yellow trace is the ambient noise floor of the measurement system and is always a good idea to record for reference. The aqua and violet traces are the two converter measurements. Note that both produce broadband noise currents out to 1 GHz, with the convertor in violet out to beyond 1.5 GHz. Note the violet trace is 20 to 50 dB higher than the ambient noise floor.



11:40:58 2015-09-16
Ref -30.00 dBm
Att 0 dB
DL -30.00 dBm
Start Freq 30.000 MHz
RBW 30.000 kHz
VBW 30.000 kHz
Stop Freq 1.5000 GHz
SWT 1.6333 s

Figure 5 - In this example, we're looking from 30 MHz to 1.5 GHz to generally characterize the spectral emissions profile of a couple of on-board DC-DC converters. Both will potentially cause interference to mobile phone bands in the 700 to 950 MHz region. The one with the violet trace is over 30 dB above the ambient noise level in the mobile phone band.

Remediation Tips – To reduce the risk of self-interference to on-board mobile phone modems and wireless systems, the product design must start off with EMC in mind and with no corners cut.

This will consist of:

- A near perfect PC board layout
- Filtering of DC-DC converters
- Filtering of any high frequency device
- Filtering of the radio module
- Local shielding around high noise areas
- Possibly shielding the entire product
- Proper antenna placement

The PC board layout is critical and is where most of your effort should reside. An eight or ten layer stack-up will provide the most flexibility in segregating the power supply, analog, digital, and radio sections and provide multiple ground return planes, which may be stitched together around the board edge to form a Faraday cage. Care must be taken to avoid return current contamination between sections – especially in the ground return planes. For wireless products, the power plane for the radio modem section should be isolated (except via a narrow bridge) from the digital power plane. All traces to this isolated plane should pass over the bridge connecting the two. This can provide up to 40 dB of isolation between the digital circuitry and radio.

It is vital that the power and ground return planes be on adjacent layers and ideally 3-4 mils apart at the most. This will provide the best high frequency bypassing. All signal layers should be adjacent to at least one solid ground return plane. Clock, or other high-speed traces, should avoid passing through vias and should not change reference planes.

Power supply sections should be well isolated from sensitive analog or radio circuitry (including antennas). Be aware of primary and secondary current loops and their return currents. These return currents should not share the same return plane paths as digital, analog, or radio circuits. Remember that high frequency return currents want to return to the source directly under the source trace.

For more details on resolving DC-DC converter noise issues with wireless radio modems, refer to *Reference 2.*

PC Board Plane Resonance and the Effect on Radiated Emissions

Noise propagation in a simple system can be represented by three elements, the voltage regulator, the printed circuit board planes with decoupling capacitors (PDN) and the device being powered (load).

Each of these three elements is comprised of resistive, inductive and capacitive terms. Even "noise free" low dropout (LDO) regulators can be highly inductive (*Reference 3*). The resistive, inductive and capacitive terms can resonate amplifying the noise signals created by the power supply and the load as they travel across the PDN creating EMI. The harmonics of the switching frequency and the switch ringing discussed earlier excite these PDN resonances (*Reference 4*). As stated previously this noise can degrade and interfere with on-board wireless modems, as well as resulting radiated and conducted emissions.

A short video helps explain the basic principles of PDN design (*Reference 5*). The radiated EMI of a LTC3880 DC-DC converter measured near the input plane using an H-field probe is seen in *Figure 6*.

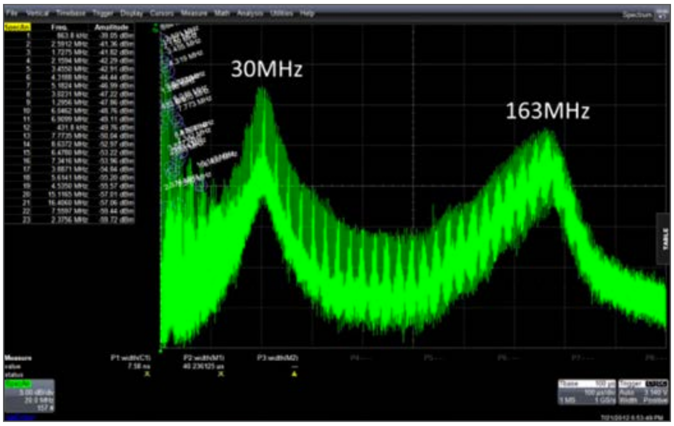


Figure 6. Spectrum analyzer display showing the 30 MHz and 160 MHz resonances detected near the input power connections of a DC-DC converter.

The 163 MHz is attributed to the ringing of the switches as seen in *Figure 7*. This ringing is caused by the inductance of the upper MOSFET bond wires, pins and circuit board planes, ringing with the lower MOSFET and PC board capacitance.

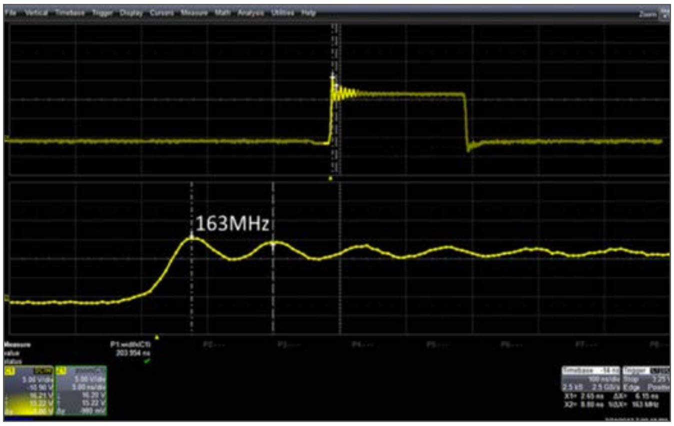


Figure 7. The 163 MHz EMI is easily explained by the ringing at the switch device, as discussed earlier.

The input ceramic decoupling capacitor resonates at approximately 30 MHz, as seen in *Figure 8* and results in the large 30 MHz EMI signature.

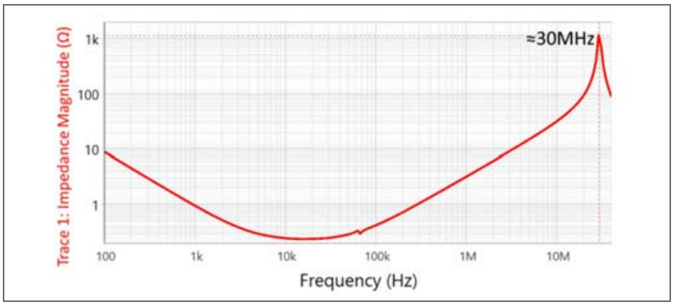


Figure 8. The larger 30 MHz emission is identified as a printed circuit board resonance using an H-field probe and confirmed by a 1-port reflection impedance measurement at the input capacitor.

The input power plane section of the DC-DC converter (measured in *Figure 6*) is shown in *Figure 9* with schematic representations of the component, PC board and external connections.

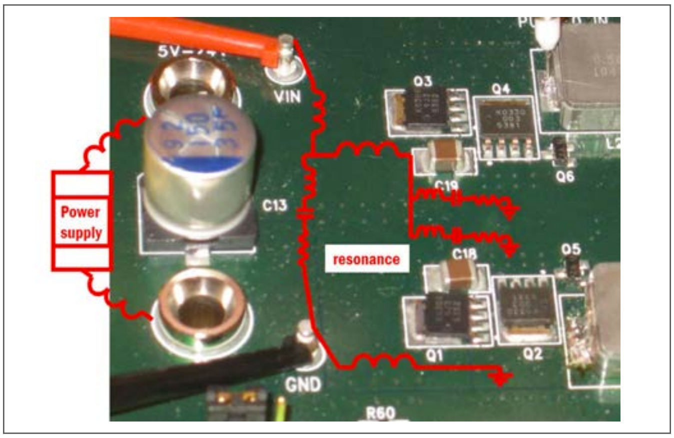


Figure 9. The power plane section of the DC-DC converter (measured in Figure 6) with schematic representations of the component, PC board and external connections.

A very simple simulation example can be used to illustrate these impedance resonance effects. Consider a simple DC-DC converter as shown in *Figure 10*.

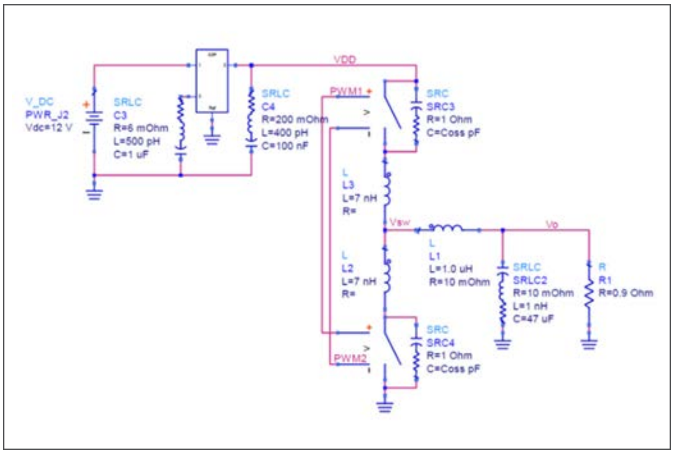


Figure 10. A simple DC-DC converter for illustration of plane resonance EMI. The "FET" switches include lead inductance and drain capacitance (Coss). A small PC board and two ceramic capacitors are included.

Designers frequently place the FET switches on one side of the board with power entry on the opposite side of the PC board. The small PC board plane used in this example has power entry through a pair of pins and no interconnect inductance is added to connect power to the PC board. A large 47 μF ceramic capacitor is placed on the top side of the PC board, while a smaller, 0.1 μF ceramic capacitor is placed very close to the FET switches on the bottom side of the PC board. Two parallel vias connect power and ground from the top side of the PC board to the bottom side as seen in *Figure 11*.

The simple model is used to simulate the harmonic current in the input connector, which is directly related to conducted and radiated emissions. Two simulations are performed; one with low ESR ceramic capacitors and the other with a lower Q controlled ESR ceramic replacing the 0.1 μF capacitor close to the FET switches. Both simulations are shown together in *Figure 12*.

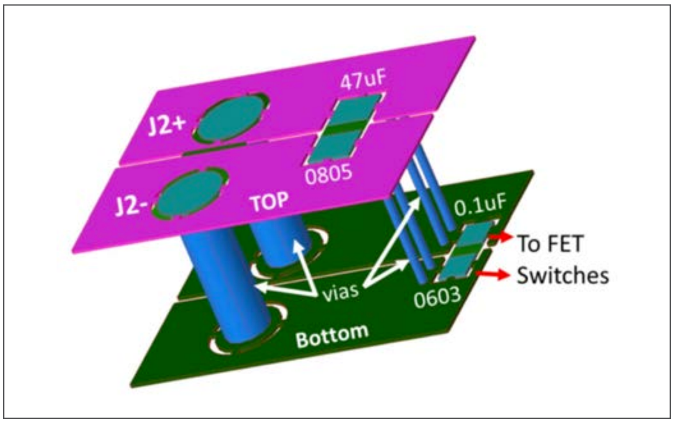


Figure 11. The large round pins on the left are the input power connector, J2. The larger capacitor on the top side is an 0805 sized 47 μF and the smaller capacitor on the bottom side is an 0603 sized 0.1 μF.

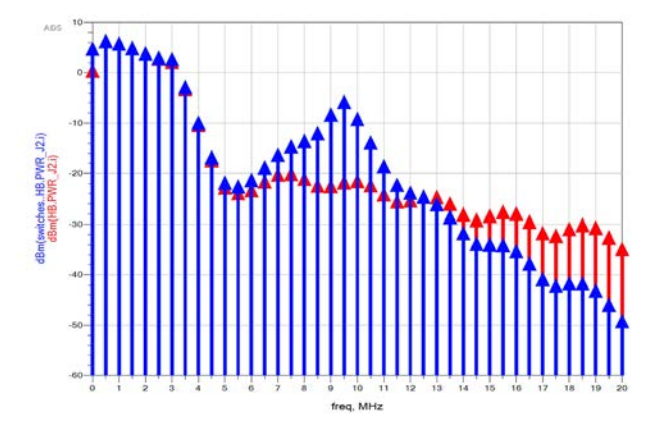


Figure 12. Spectral simulation of the input power lead shows the high Q ceramic (10 mΩ blue) has a clear peak near 10 MHz that is eliminated using a controlled ESR ceramic (200 mΩ red)

The simulated impedance, measured at the smaller capacitor in *Figure 13* shows the corresponding plane resonance with a clear 10 MHz peak using the high Q ceramic capacitor (blue) and the peak is eliminated using the controller ESR ceramic capacitor (red).

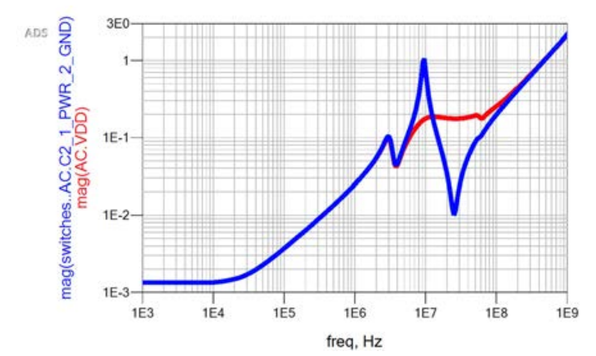


Figure 13. The simulated impedance at the 0.1 uF capacitor using high Q ceramic (10 mΩ blue) and a controlled ESR ceramic (200 mΩ red)

Remediation Tips – To minimize PDN resonances, the complete system of voltage regulator, PDN and the load need to be carefully balanced. Damping resistance must be included to eliminate or minimize the existence or Q of resonances. This will consist of:

- Short, wide power planes
- Keep the layout as small as possible to minimize inductance
- Thinner PC board dielectric layers, closer to the surface
- Incorporate EM simulation to identify and minimize PDN resonances
- Keep capacitors on one side of the PC board to the extent possible
- Low-Q or ESR controlled capacitors reduce Q
- Choose voltage regulators and output capacitors for good control loop stability
- Don't place cutouts or holes in ground plane layers below the power plane

- Ferrite beads are a very common cause of PDN resonances
- Be aware of inductive interconnects bringing power to the system.

Printed circuit board design and decoupling is critical and “rules-of-thumb” generally don’t work well in high speed circuits. The design of the circuit board and capacitor decoupling always involves trade-offs, but the impacts on resonances need to be weighed carefully. A multi-frequency harmonic comb generator can be extremely helpful for quickly identifying PDN resonances (*Reference 3*).

Summary

As you can see, designing DC-DC converters, LDOs, and PDNs with today’s high-speed technology nearly always requires careful circuit design, adequate filtering, simulation of the PDN, very careful circuit board layout, and use of controlled-ESR filter capacitors. Poor designs can result in:

- Ringing in power supply switches (or other fast-edged digital switching) resulting in associated radiated or conducted emissions resonant peaks at the ring frequency and harmonics.
- High frequency broadband noise well beyond 1 GHz, resulting in self-interference to radio modems.
- Poor stability and resonances in un-damped power distribution networks, leading to instability, spectral resonances, and associated radiated and conducted emissions.

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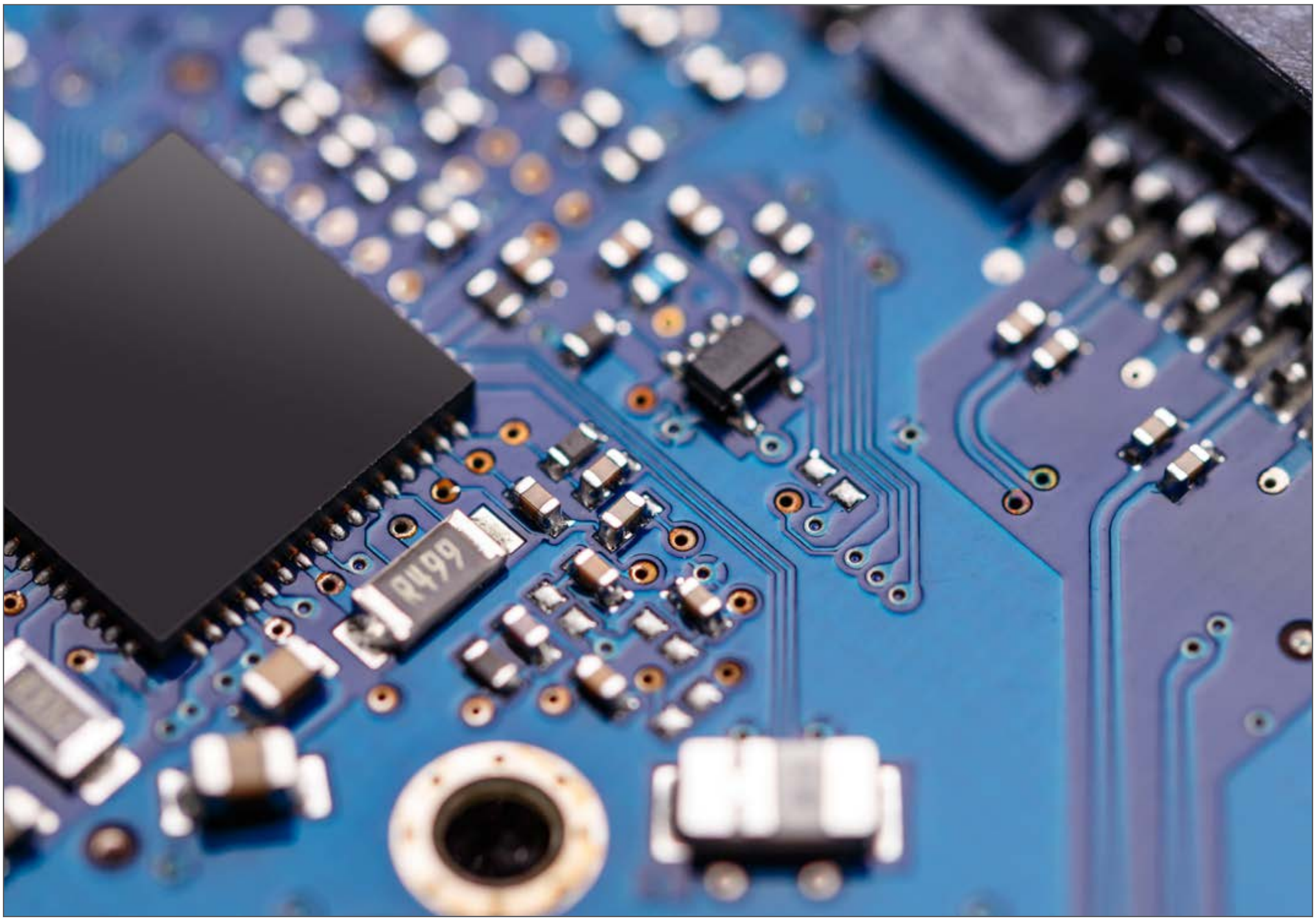

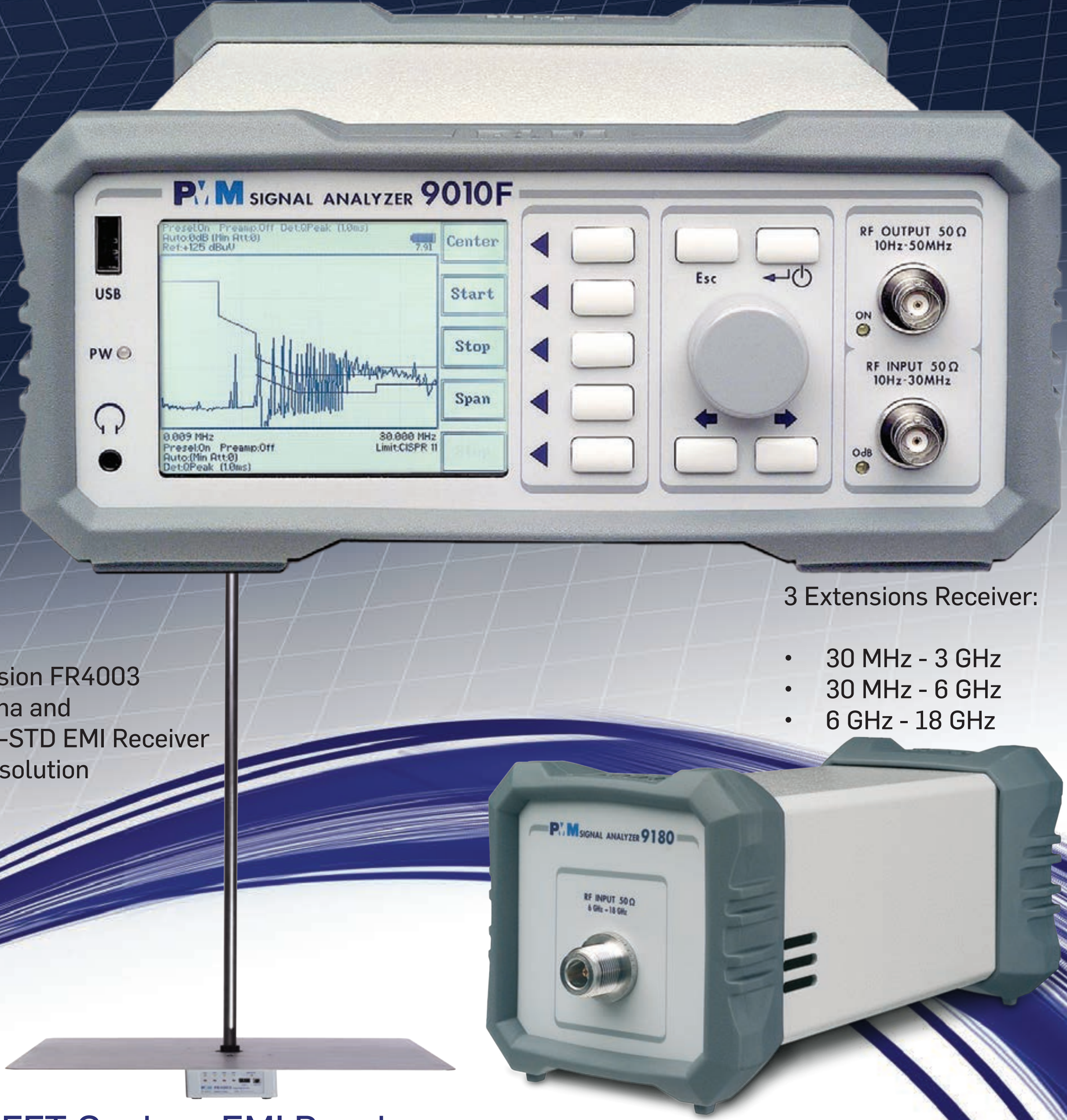
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PW
Center
Start
Stop
Span
Esc
RF OUTPUT 50Ω 10Hz-50MHz
ON
RF INPUT 50Ω 10Hz-30MHz
0dB
PMM SIGNAL ANALYZER 9180
RF INPUT 50Ω 6 GHz - 18 GHz

DOES YOUR AUTOMOTIVE PRINTED CIRCUIT BOARD HAVE TOO MANY GROUNDS?

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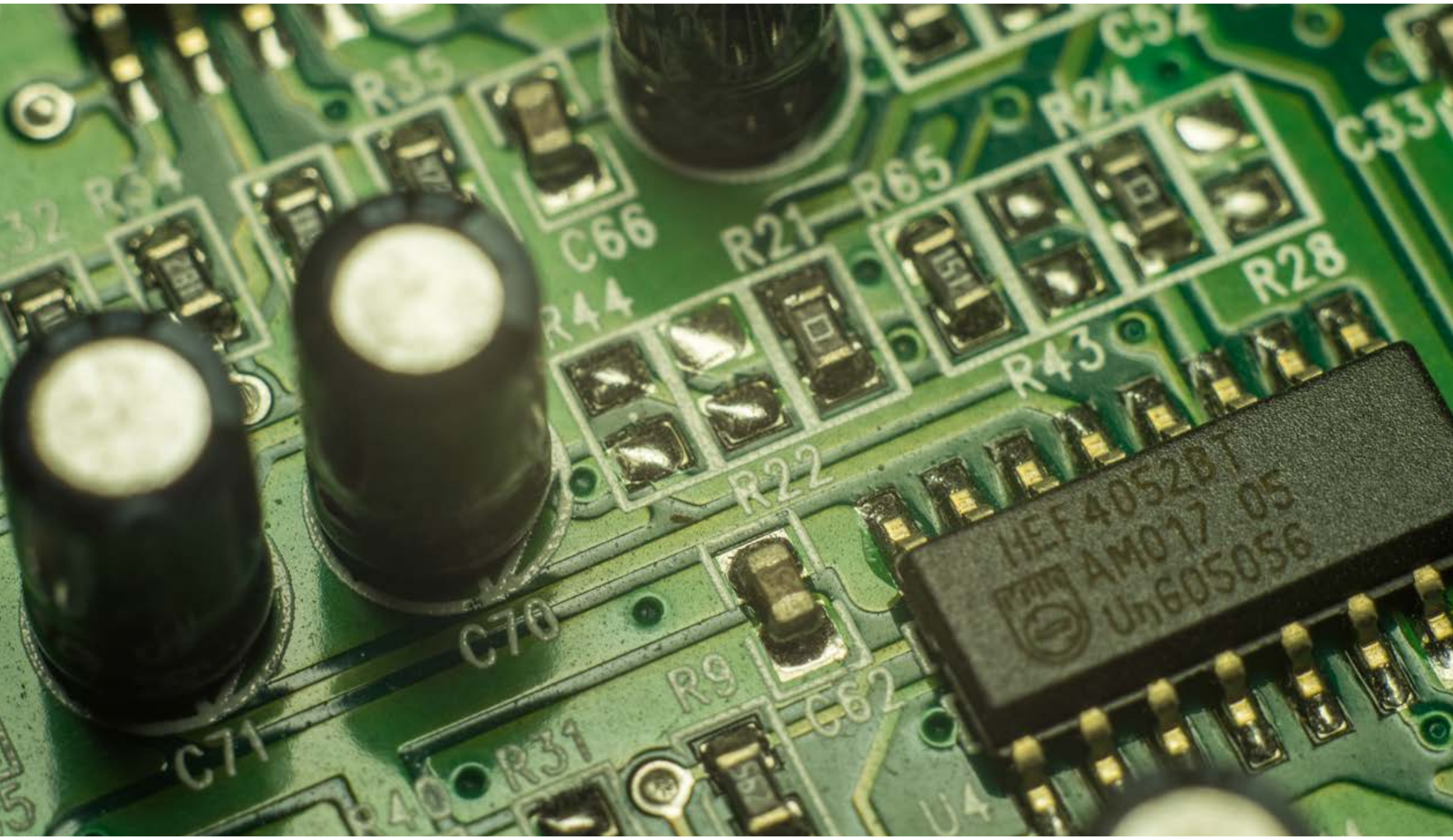


DOES YOUR AUTOMOTIVE PRINTED CIRCUIT BOARD HAVE TOO MANY GROUNDS?

Abstract

One of the most widespread design defects in automotive printed circuit boards is the lack of an established high-frequency reference ground. This problem is exacerbated by a tendency among automotive design engineers to cut up solid current return planes in an attempt to establish “noisy” and “quiet” grounds.

Introduction

Too often, the designers of automotive electronic systems shoot themselves in the foot (so to speak), making design decisions that ultimately make it difficult for their products to meet the automotive EMC requirements. Basic design flaws such as improper grounding, poor trace routing, and ineffective decoupling are widespread throughout the industry. Many designs also fail to control the routing of currents induced by immunity tests such as bulk current injection or electrical fast transient testing.

Historically, the significance of these design flaws has been diminished by relatively long development cycles that allowed a test-and-fix design strategy. EMC problems that couldn’t be fixed were often dealt with by waiving the requirement. Today however, a growing number of electronic systems play a critical role in automotive safety. There is no opportunity to experiment with multiple iterations of the hardware design during development; and waivers of EMC requirements are becoming harder to obtain.

This article addresses one of the most widespread and damaging design flaws in automotive printed circuit boards today, the lack of a single high-frequency ground reference. More specifically, there is a tendency among automotive circuit board designers to over-partition their “ground” planes.

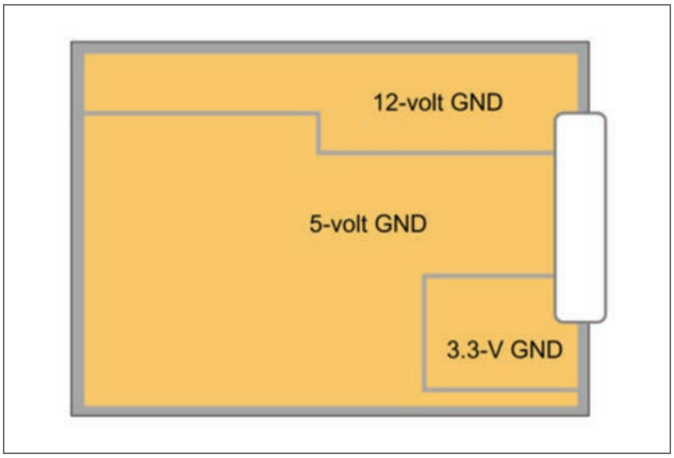


Figure 1. A circuit board with isolated “grounds” for 12-volt, 5-volt and 3.3-volt components.

What’s the Problem?

It is not uncommon for an automotive circuit board to have multiple “grounds”. For example, as illustrated in *Figure 1*, there may be one ground for the 12-volt devices, one ground for the 5-volt devices, and a separate ground for the 3.3-volt digital logic. It is also not uncommon to see isolated grounds for analog sensors, power supplies, motor drivers, memory devices or anything else that is considered particularly noisy or susceptible to noise. Decisions to isolate various grounds are motivated by a desire to reduce interference between various circuits on the board. Usually, this is done without any attempt to quantify the amount of interference that would have resulted if the grounds had not been isolated (even though this is a simple calculation).

The problem with isolating the voltage references (ground) of various circuits on a printed circuit board is illustrated in *Figure 2*. Isolated grounds are not held to the same potential, i.e. there is likely to be a voltage difference between them. That means there is likely to be a voltage difference between circuits referenced to different grounds. If those circuits communicate with each other on the board, that voltage difference appears as noise on the signals. If those circuits communicate with circuits off the board, then wires leaving the board have a voltage difference between them.

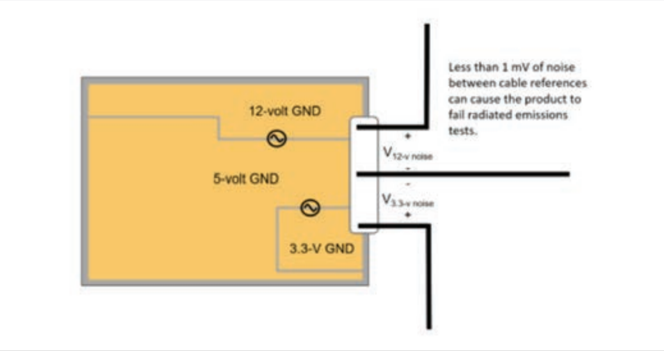


Figure 2. Illustration of the voltage differences between “grounds” driving unpaired wires in a harness.

At frequencies where radiated emissions are likely to be a concern, a voltage as low as 1 mV between unpaired wires in a wiring harness can result in EMC test failures. [In some frequency bands, 0.1 mV is sufficient to cause a failure.] In order to ensure that a design complies with radiated emissions requirements (and for similar reasons, radiated immunity requirements), it is extremely important to maintain a single RF ground reference for every circuit connected to a wiring harness. Ensuring that all of the wires in a harness are held to the same potential (within 0.1 mV) at RF frequencies is relatively straightforward in a design with a single solid ground plane; but it can be extremely difficult in boards with isolated grounds.

Why Isolate Grounds?

If isolating grounds is such a bad practice, why are so many boards designed that way? Often, the answer is that the designers were following the advice of a component supplier's application note, or they were simply mimicking the design of a product that had been successful in the past. There is one valid reason that a board designer might not want to let two circuits share the same ground plane. That is to prevent common-impedance coupling. Common-impedance coupling (or conducted coupling) occurs when two circuits share parts of their current paths. Currents from the circuit behaving as the noise source flowing in the shared part induces a voltage in both circuits. For example the two circuits represented schematically in *Figure 3* share the same current return path. The impedance of that return path is RRET. If Circuit 1 (the outer loop) creates a current, IRET, flowing in the return path, then a voltage is developed across the return path, VRET = IRET RRET. By Kirchhoff's voltage law, some of this voltage will appear across the Circuit 2 source, and the rest will appear across the Circuit 2 load.

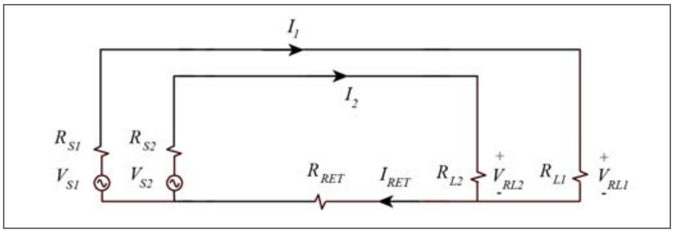


Figure 3. Two circuits sharing the same current return conductor.

Common-impedance coupling is one of four EM coupling mechanisms, along with electric-field coupling, magnetic-field coupling and radiation coupling. Common-impedance coupling is most likely to be important at relatively low frequencies when the source circuits have relatively low impedance. The two most common methods for reducing common-impedance coupling are to reduce the impedance of the shared part of the circuit, or to isolate the circuits so that they don't share a current path.

Providing separate "grounds" for various circuits on a circuit board is one method for reducing the common-impedance coupling between these circuits. This can be effective if high-current circuits use the ground plane as part of their current return path, and if that path is shared by circuits sensitive to small noise voltages. It is important to note that isolating current-return paths by partitioning a solid copper plane is only effective for reducing common-impedance coupling. The other EM coupling mechanisms are generally not affected by partitioning the return plane. In fact, gapping a solid ground plane can actually increase the electric and magnetic field coupling between traces routed over different portions of the plane.

When Should Current Returns be Isolated?

Designs that isolate current return conductors are justified when common-impedance coupling is a significant concern. Unlike high-frequency currents, low-frequency (e.g. below 100 kHz) currents flowing on a printed circuit plane will spread out. This means that all circuits that use a "ground" plane to return low-frequency currents share a portion of their current paths.

In these situations, it's relatively easy to quantify the maximum possible common-impedance coupling. The maximum possible voltage coupled to a victim circuit is equal to the maximum resistance of the plane times the maximum current produced by the source circuit. For example, consider the two circuits illustrated in *Figure 4*. A 3.3-volt digital signal shares the same current return plane as an actuator signal that can switch from 0 amperes to 10 amperes in less than 1 microsecond. To calculate the maximum possible common-impedance coupling, we'll assume that the traces are near each other and calculate the coupling that would occur if they both ran the entire length of the board.

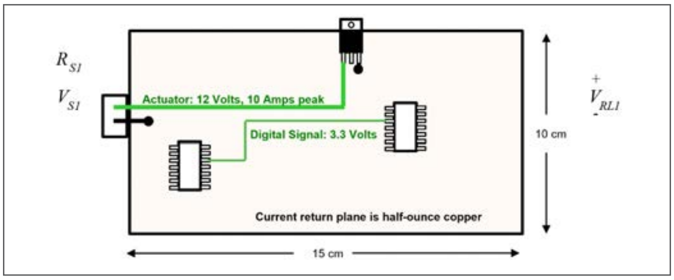


Figure 4. Two circuits sharing the same current return plane.

Since the plane is half-ounce copper (~17.8 µm thick), it has an end-to-end resistance of approximately,

$$\begin{aligned} R &= \frac{\quad}{\sigma A} \\ &= \frac{0.15\ \text{m}}{(5.8\times 10^{7}\,\text{S/m})(0.10\,\text{m})(17.8x10^{-6}\text{m})} = 1.5\ \text{m}\Omega \end{aligned} \quad (1)$$

Therefore, the maximum coupled voltage due to common-impedance coupling is,

$$\begin{aligned} V_{coupled} &\leq (1.5\times 10^{-3}\,\Omega)(10\,\text{A}) \\ &\leq 15\,\text{mV} \end{aligned} \quad (2)$$

Clearly, in this case, it is ok to allow these two signals to share the same current return plane. In fact, a few amperes of low-frequency current will generally translate to a few millivolts in a printed circuit board ground plane; so it is rarely necessary to provide an isolated return plane.

In rare situations where a calculation shows that low-frequency isolation is necessary, it is usually better to route the source or victim return currents on traces that occupy a different layer leaving the ground plane undivided. Generally, if two large grounds are isolated at low frequencies, they must still be connected at high frequencies in order to avoid radiated emissions and radiated immunity issues. Routing current returns on different layers facilitates their connection at high frequencies using capacitors with low connection inductance.

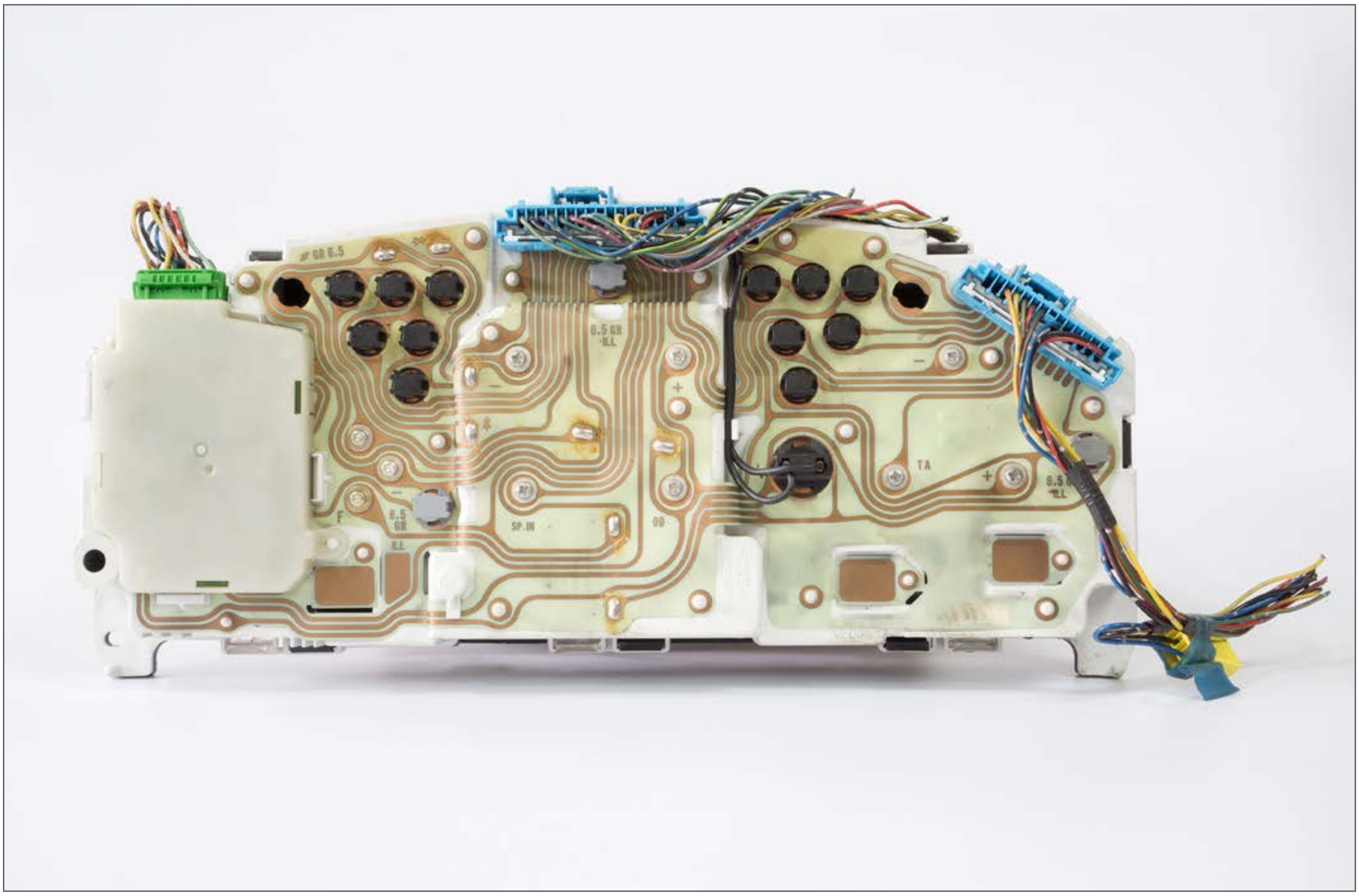
The fact that the current switched in less than 1 microsecond was not a factor in this calculation. That's because the dominant common impedance at low frequencies is the resistance of the plane. The coupled voltage waveform will mimic the shape of the source current waveform and the amount of common-impedance coupling will not depend on the rate of change of the signal. In the example above, electric-field and/or magnetic-field coupling would certainly be a significant concern. The field coupling would make it necessary to separate these traces. Nevertheless, it is critical to note that isolating the actuator's return plane from the digital signal's return plane would NOT significantly reduce the electric or magnetic field coupling.

Does Your Board Have Too Many Grounds?

It typically requires hundreds of millivolts of noise in order to interfere with digital logic. So unless the interfering circuits are switching hundreds of amperes of current, it is generally fine to allow these circuits to share a current return plane. Likewise digital logic, which typically switches peak currents on the order of hundreds of milliamps, can readily share a return plane with analog circuits capable of tolerating a few hundred microvolts of induced noise. Simple common-impedance coupling calculations like those in (*1*) and (*2*), will tell you if you need to isolate your current return paths at low frequencies.

At frequencies above 100 kHz, currents returning on a plane are concentrated beneath the signal trace. Common-impedance coupling is easily avoided by providing separation between the signal traces. Separating the traces is also generally effective for reducing electric and magnetic field coupling, which are much more likely to be the dominant coupling mechanisms at high frequencies.

A good rule of thumb when laying out automotive printed circuit boards is, "Never gap a solid ground plane." In situations where it is necessary to isolate low-frequency return currents, route the return currents of either the source or the victim circuits on a different layer. This will make it easier to re-establish a connection between these "grounds" at high frequencies in order to meet radiated emissions and immunity requirements.



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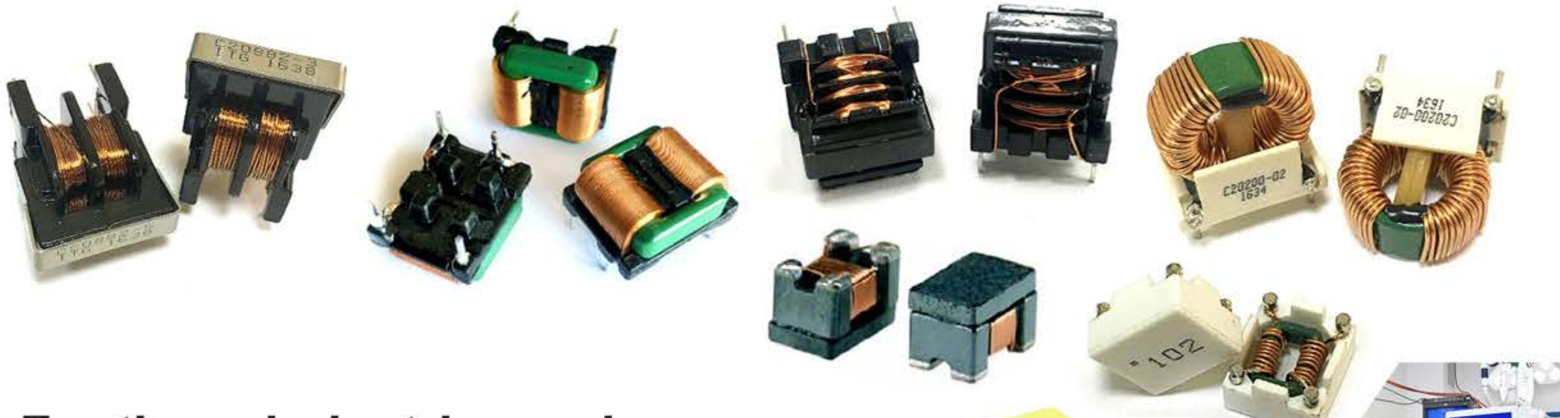

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AUTOMOTIVE EMC TEST LABS

If your test lab specializes in automotive EMC testing and is not listed, please contact:
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and we'll include you in the next issue.

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http://www.cetecom.com/en/products-services/testing.html

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MET Laboratories
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https://www.tuv-sud-america.com/us-en

Underwriters labs
http://services.ul.com/service/emc-automotive-testing/

Yazaki Testing laboratory
http://www.yazakiemc.com/wp/

AUTOMOTIVE INDUSTRY GROUPS

Auto Alliance
http://www.autoalliance.org

Automotive Industry Action Group
http://www.aiag.org

European Automobile Manufacturers Association
http://www.acea.be

National Automobile Dealers Association
https://www.nada.org

Automotive Council UK
http://www.automotivecouncil.co.uk

Eclipse Automotive Working group
http://www.eclipse.org/org/workinggroups/autowg.php

Automotive Industries Association of Canada
https://www.aiacanada.com

Center for Automotive Research
http://www.cargroup.org

German Association of the Automotive Industry
https://www.vda.de/en

Motor Trades Association of Australia
http://www.mtaa.com.au

Shanghai Automotive Industry Corporation
http://www.chinacsrmap.org/index_CN.asp

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http://www.cvel.clemson.edu/auto/index.html
http://www.cvel.clemson.edu/emc/index.html

MAGAZINES

Vehicular Technology Magazine, IEEE
IEEE Vehicular Technology Magazine publishes peer-reviewed articles covering advances in areas of interest to the IEEE Vehicular Technology Society: The theoretical, experimental, application and operational aspects of electrical and electronic engineering relevant to motor vehicles and associated land transportation infrastructure.

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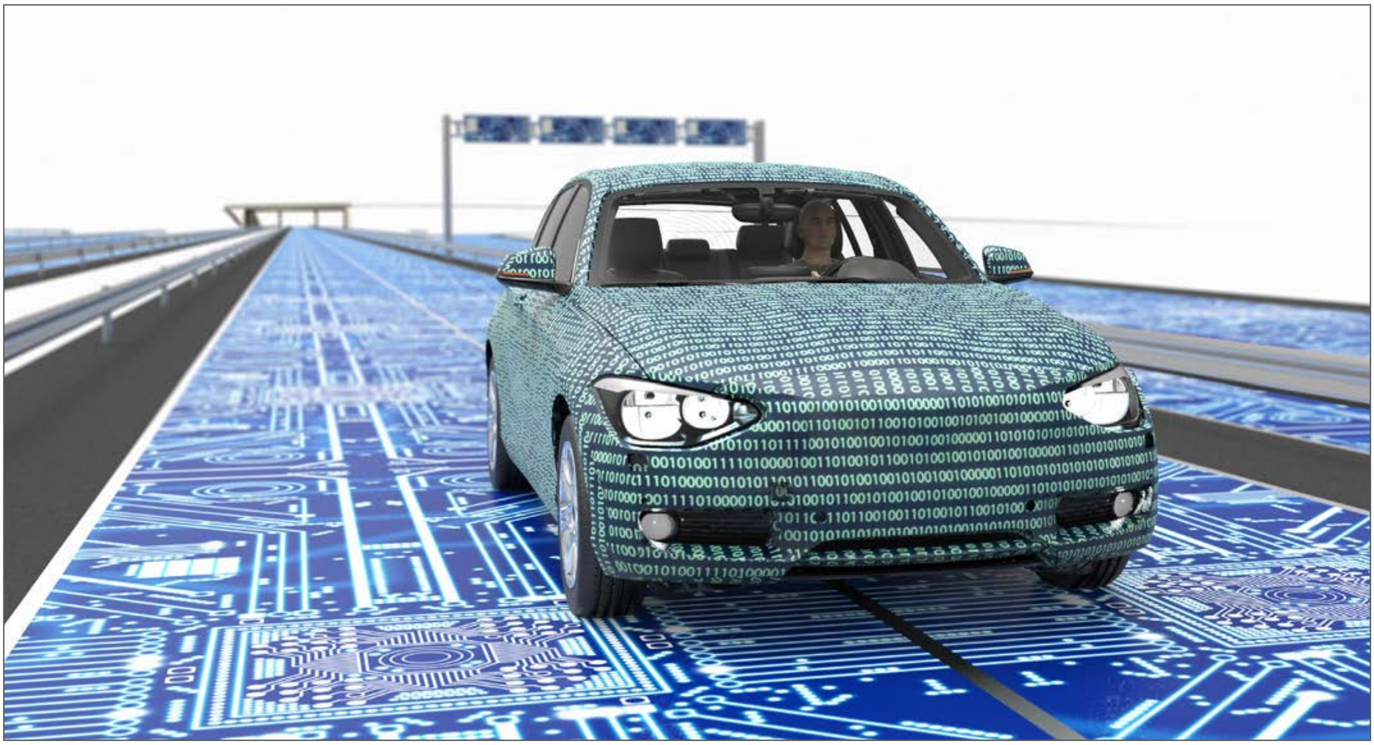

AUTOMOTIVE EMC CONFERENCES

The following is a partial listing of major automotive electronics conferences planned for 2017 and 2018. If your conference is not listed, please contact: info@interferencetechnology.com

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AUTOMOTIVE ELECTRONICS CONFERENCES

European Battery, Hybrid & Fuel Cell Electric Vehicle Congress
March 14-16, 2017
Geneva, Switzerland
http://www.eevc.eu

The European Electric & Hybrid Vehicle Congress is a global platform to foster exchange of views between the R&D, the industry, the authorities, and end users to develop synergies in the field of e-mobility.

Vehicle Technology Conference (VTC)
September 24-27, 2017
Toronto, Canada
http://www.ieeevtc.org/vtc2017fall/

VTC will bring together individuals from academia, industry and government to discuss and exchange ideas in the fields of mobile, wireless and vehicular technology as well as the applications and services associated with such technology. Features include world-class plenary speakers, panel sessions, tutorials, and both technical and application-based sessions.

Electric & Hybrid Vehicle Technology Show
September 12-14, 2017
Novi, MI
http://www.evtechexpo.com

Electric & Hybrid Vehicle Technology Expo is the premier showcase for electric and hybrid vehicle technology and innovation. The show highlights advances right across the powertrain and across a wide range of vehicles from passenger and commercial to off-highway industrial vehicles.

The Battery Show - North America
September 12-14, 2017
Novi, MI
https://www.thebatteryshow.com

The Battery Show 2017 is the premier showcase of the latest advanced battery technology.

Automotive Test Expo
October 24-26, 2017
Novi, MI
http://www.testing-expo.com/usa/

This conference includes the very latest technologies and services that are designed to ensure that the highest standards are met in terms of product quality, reliability, durability and safety.

Applied Power Electronics (APEC)
March 4-8, 2018
San Antonio, Texas
http://www.apec-conf.org

APEC focuses on the practical and applied aspects of the power electronics business. This is not just a designer's conference; APEC has something of interest for anyone involved in power electronics:

- Equipment OEMs that use power supplies and dc-dc converters in their equipment
- Designers of power supplies, dc-dc converters, motor drives, uninterruptable power supplies, inverters and any other power electronic circuits, equipment and systems
- Compliance engineers testing and qualifying power electronics equipment or equipment that uses power electronics

The Battery Show - Europe
May 15-17, 2018
Hanover, Germany
https://www.thebatteryshow.com

The Battery Show Europe Exhibition & Conference is a showcase of advanced battery manufacturing and technology for electric & hybrid vehicles, utility & renewable energy support, portable electronics, medical technology, military and telecommunications.

Global Automotive Components and Suppliers
June 5-7, 2018
Stuttgart, Germany
http://www.globalautomotivecomponentsandsuppliersexpo.com/en/

Automotive Component Manufacturers from around the world will be at the expo to display their very latest technologies and products, plus numerous more exhibitors will be on hand to discuss how they can participate in cost reduction within supply chains, and how they can offer new, alternative, cost-effective manufacturing and supply solutions.

AUTOMOTIVE EMC CONFERENCES (CONTINUED)

Automobil Elektronik Kongress
June 19-20, 2018
Ludwigsburg, Germany
https://www.automobil-elektronik-kongress.de/en/registration/#registrati

The International Congress on Advances in Automotive Electronics once again proved to be a magnet with considerable influence on decision-makers in electrical/electronic system development for the vehicle industry.

2017 SAE CONFERENCES

Symposium on International Automotive Technology 2017
January 18-21, 2017
Pune, India
https://siat.araiindia.com

The Symposium on International Automotive Technology (SIAT) is a benchmark event organized by ARAI biennially. SIAT serves as an important forum for exchange of ideas and brainstorming for the automotive industry. Over the years, the event has grown in stature and is now considered as a prestigious automotive event in the global automotive fraternity.

SAE 2017 On-Board Diagnostics Symposium - Europe
February 27-March 1, 2017
Torino, Italy
http://www.sae.org/events/obd-eu/

This automotive and commercial vehicle event delivers both insight into, and subsequent engineering reaction to, the latest CARB, EPA, and EC requirements and regulations, as well as details of the associated SAE standards regarding light- and heavy-duty emissions controls.

SAE 2017 North American International Powertrain Conference
September 13-15, 2017
Chicago, Illinois, USA
http://saeevents.org/events/sae-2017-north-american-international-powertrain-conference

The SAE 2017 North American International Powertrain Conference (NAIPC) invites executives from the automotive industry to discuss and debate the most profound issues in the North American powertrain market.

SAE 2017 On-Board Diagnostics Symposium
September 26-28, 2017
Garden Grove (Anaheim), California, USA
http://www.sae.org/events/obd/2017/

This event serves as the platform for uniting automotive and commercial vehicle industry experts who need information and insight into CARB, EPA, and EURO IV/V/VI rules and regulations, and SAE standards associated with light- and heavy-duty emissions controls.

SAE 2018 Connect to Car
January 8, 2018
Las Vegas, Nevada
http://www.sae.org/events/c2c/

Join us for the SAE International conference track at CES® 2017. The 2017 program is bigger and better than anything we have done at CES®! We have partnered with the GENIVI Alliance to create a full-day program that brings the best of current automotive technology discussions to CES®!

SAE 2017 Hybrid and Electric Vehicle Technologies Symposium
February 20-22, 2018
San Diego, California
http://www.sae.org/events/hybridev/

The SAE 2017 Hybrid & Electric Vehicle Technologies Symposium is the source for current and forward-looking hybrid and electric vehicle technology advances, providing industry developments from prominent representatives of OEM and supplier companies.

AUTOMOTIVE EMC CONFERENCES (CONTINUED)

OTHER CONFERENCES THAT INCLUDE AUTOMOTIVE EMC

International Exhibition with Workshops on Electromagnetic Compatibility EMC (EMV 2018)
February 20-22, 2018
Duesseldorf, Germany
https://www.mesago.de/en/EMV/home.htm?ovs_tnid=0

EMV is Europe's leading event on electromagnetic compatibility. Meet the industry's leading companies for EMC-equipment, components and EMC-services. The event offers a wide range of EMC-specific topics. The perfect platform to get the latest information on newest trends and developments!

The 2017 Symposium on EMC+SIPI
August 7-11, 2017
National Harbor, Maryland
http://www.emc2017.emcss.org

2018 Joint IEEE International Symposium on EMC and APEMC
May 14-15, 2018
Singapore Er Ping Li, erpingli@ieee.org
http://www.emcs.org/conferences_main.html

The 2018 Symposium on EMC+SIPI
July 30 - August 3, 2018
Long Beach, California Ray Adams, r.k.adams@ieee.org
http://www.emcs.org/conferences_main.html

The Symposium on EMC, SI & PI is the leading event to provide education of EMC and Signal and Power Integrity techniques to specialty engineers. The Symposium features five full days of innovative sessions, interactive workshops, tutorials, experiments, demonstrations, and social networking events.

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